



# ANNAI VAILANKANNI COLLEGE OF ENGINEERING

(A Christian Minority Institution)

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

Recognized under section 2(f) of UGC Act 1956

Website: [www.avce.edu.in](http://www.avce.edu.in)

## AUTHENTICATION CERTIFICATE

Mechanism of internal/ external assessment is transparent and the grievance redressal system is time- bound and efficient.

The list of following documents enclosed

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**PRINCIPAL**  
**ANNAI VAILANKANNI COLLEGE OF ENGINEERING**  
**POTTALKULAM**  
**AZHAGAPPAPURAM - 629 401**  
**KANYAKUMARI DIST.**



Address:  
AVK Nagar, Pottalkulam,  
Azhagappapuram Post, Kanyakumari District - 629401.



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Date: 02.11.2022



**CENTRE FOR ACADEMIC COURSES**

ANNA UNIVERSITY: : CHENNAI – 600 025

**ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES**

**November 2022 – April 2023 (SEMESTER I)**

UG (FT/PT) Degree Programmes

Sl. No.	Programme	Semester	Commencement of Induction Programme	Commencement of Classes	Last working day	Commencement of Practical Examinations	Commencement of End Semester Examinations
1.	B.E. / B.Tech. (Full Time)	I	14.11.2022	28.11.2022	23.03.2023	25.03.2023	05.04.2023
2.	B.Arch.(Full Time)	I	14.11.2022	28.11.2022	15.03.2023	25.03.2023	05.04.2023
3.	B.E. / B.Tech. (Part Time)	I	-	14.11.2022	01.03.2023	25.03.2023	05.04.2023

RE-OPENING DAY FOR THE NEXT SEMESTER: 15.05.2023 (Monday)

**NOTE:**

1. The Theory and Practical Examination schedules will be published in due course. (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

  
PRINCIPAL  
ANIM WILASWAMI COLLEGE OF ENGINEERING  
FOTTALETHAN  
AZHAGAPPAPURAM - 605 001  
SANTHOSHAPURAM DIST.

  
DIRECTOR  
ACADEMIC COURSES

Date: 02.11.2022

**REVISED - I****CENTRE FOR ACADEMIC COURSES**

ANNA UNIVERSITY: CHENNAI - 600 025

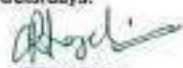
**ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES****August 2022 – December 2022 (Semester III)**

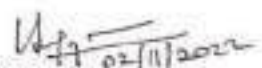
UG (FT/PT) &amp; PG (FT/PT) Degree Programmes

Sl. No.	Programme	Semester	Commencement of Classes	Last working day		Commencement of Practical Examinations		Commencement of End Semester Examinations	
				Existing	Revised	Existing	Revised	Existing	Revised
1.	B.E / B.Tech. (Full-Time)	III	22.08.2022	08.12.2022	27.12.2022	10.12.2022	18.01.2023	21.12.2022	29.12.2022
2.	B.Arch. (Full-Time)	III	22.08.2022	08.12.2022	-	10.12.2022	18.01.2023	21.12.2022	29.12.2022
3.	B.E / B.Tech (Part-Time)	III							
4.	M.B.A. (5 Yrs-Integrated)	III							
5.	M.B.A. (Full-Time & Part-Time)	III	01.09.2022	19.12.2022	-	21.12.2022	18.01.2023	02.01.2023	29.12.2022

**RE - OPENING DAY FOR THE NEXT SEMESTER: 01.02.2023 (Wednesday)****NOTE:**

1. The Theory and Practical Examination schedules will be published in due course (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

  
**PRINCIPAL**  
 ANNA VARADANATHI COLLEGE OF ENGINEERING  
 POTTALKULAM  
 AZHAGAPPAPURAM - 600 601  
 KANNIYAKUMARI DIST.

  
**DIRECTOR**  
 ACADEMIC COURSES

DAC - 08

Date: 02.11.2022

**REVISED****CENTRE FOR ACADEMIC COURSES**

ANNA UNIVERSITY: : CHENNAI – 600 025

**ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES****August 2022 – December 2022 (ODD SEMESTER – Except Semester III)**UG Programmes

Sl. No	Programme	Semester	Commencement of Classes	Last working day		Commencement of Practical Examinations		Commencement of End Semester Examinations	
				Existing	Revised	Existing	Revised	Existing	Revised
1.	B.E. / B.Tech (Full-Time)	V, VII	10.08.2022	19.11.2022	06.12.2022**	21.11.2022	18.01.2023	01.12.2022	08.12.2022
2.	B.E. / B.Tech (Part-Time)	V, VII	10.09.2022	19.11.2022	-	21.11.2022	-	01.12.2022	-
3.	B.Arch. (Full-Time)	V, VII, IX							

**RE - OPENING DAY FOR THE NEXT SEMESTER: 30.01.2023 (Monday)****NOTE:**

- The Theory and Practical Examination schedules will be published in due course (Practical Examinations will be conducted before the theory examinations).
- If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

\*\* In order to ensure minimum no. of working days, the following Saturdays are declared as working days.

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
1.	20.08.2022	Monday
2.	03.09.2022	Friday
3.	17.09.2022	Wednesday
4.	15.10.2022	Tuesday
5.	29.10.2022	Wednesday

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
6.	05.11.2022	Monday
7.	12.11.2022	Tuesday
8.	19.11.2022	Wednesday
9.	26.11.2022**	Thursday
10.	03.12.2022**	Friday

*[Signature]*  
**PRINCIPAL**  
 ANNA WALABESHI COLLEGE OF ENGINEERING  
 POTTAI HILLAM  
 AZHAGAPAPURAM - 609 401  
 KANNIYAKUMARI DIST.

*[Signature]*  
**DIRECTOR**  
 ACADEMIC COURSES

DAC - 02

Date: 06.10.2022



**CENTRE FOR ACADEMIC COURSES**  
**ANNA UNIVERSITY : CHENNAI - 600 025**  
**ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES**  
**October 2022 - February 2023 (Odd Semester - Semester I)**

**PG (FT) Degree Programmes**

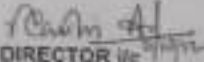
Sl. No	Programme	Semester	Commencement of Classes	Last working day	Commencement of Practical Examinations	Commencement of End Semester Examinations
1.	M.E. / M. Tech. / M. Arch.(FT)	I	10.10.2022	25.01.2023	27.01.2023	06.02.2023

**RE-OPENING DAY FOR THE NEXT SEMESTER: 08.03.2023 (Wednesday)**

**NOTE:**

1. The Theory and Practical Examination schedules will be published in due course. (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

  
PRINCIPAL  
ANNA UNIVERSITY COLLEGE OF ENGINEERS  
POTTAI KOTTAI  
AZHAGAPPAPURAM-607 401  
KANNIYAKUMARI DIST.

  
DIRECTOR /c  
ACADEMIC COURSES

Date: 02.11.2022

**CENTRE FOR ACADEMIC COURSES**

**ANNA UNIVERSITY : CHENNAI - 600 025**

**ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES**

**December 2022 - April 2023 (Odd Semester - Semester III)**

**PG (FT) Degree Programmes**



Sl. No	Programme	Semester	Commencement of Classes	Last working day	Commencement of Practical Examinations	Commencement of End Semester Examinations
1.	M.E. / M. Tech. / M. Arch.(FT)	III	12.12.2022	23.03.2023	25.03.2023	05.04.2023

**RE-OPENING DAY FOR THE NEXT SEMESTER: 15.05.2023 (Monday)**

\*\* In order to ensure minimum no. of working days, the following Saturdays are declared as working days.

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
1.	24.12.2022	Monday
2.	07.01.2023	Tuesday
3.	21.01.2023	Wednesday

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
4.	04.02.2023	Wednesday
5.	18.02.2023	Friday

1. Theory and Practical Examination schedules will be published in due course. (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

PRINCIPAL  
ANNA VELAYUTHAN COLLEGE OF ENGINEERING  
POTTALMULAM  
AZHAGAPPAPURAM - 605 001  
KANYAKUMARI DIST.

DIRECTOR  
ACADEMIC COURSES

DAC - 58

Date: 04.05.2023



**CENTRE FOR ACADEMIC COURSES**  
**ANNA UNIVERSITY: : CHENNAI - 600 025**  
**ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES**  
**May 2023 - August 2023 (Even Semester)**  
**UG (FT/PT) & PG (FT) Degree Programmes**

Sl. No.	Programme	Semester	Commencement of Classes	Last working day	Commencement of Practical Examinations	Commencement of End Semester Examinations
1.	B.E. / B.Tech. (Full-Time)	II	10.05.2023	07.08.2023**	09.08.2023	21.08.2023
2.	B.Arch. (Full-Time)	III				
3.	B.E. / B.Tech. (Part-Time)	II				
4.	M.E. / M. Tech. / M. Arch. (FT)	IV				

**RE - OPENING DAY FOR THE NEXT SEMESTER: 11.09.2023 (Monday)**

**NOTE:**

1. The Theory and Practical Examination schedules will be published in due course (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

\*\* In order to ensure minimum no. of working days, the following Saturdays are declared as working days.

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed	Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
1.	13.05.2023	Friday	7.	24.06.2023	Monday
2.	20.05.2023	Monday	8.	01.07.2023	Tuesday
3.	27.05.2023	Tuesday	9.	08.07.2023	Wednesday
4.	03.06.2023	Wednesday	10.	15.07.2023	Thursday
5.	10.06.2023	Thursday	11.	22.07.2023	Friday
6.	17.06.2023	Friday	12.	05.08.2023	Monday

*[Signature]*  
**PRINCIPAL**  
**ANNA WILAKKANI COLLEGE OF ENGINEERING**  
**POTTAIKULAM**  
**AZHAGAPPURAM - 605 401**  
**ILANKUMAM DIST.**

*[Signature]*  
**DIRECTOR**  
**ACADEMIC COURSES**

DAC - 55

Date: 30.03.2023

**CENTRE FOR ACADEMIC COURSES**  
**ANNA UNIVERSITY: CHENNAI - 600 025**

**REVISED**



**ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES**  
**February 2023 – June 2023 (Even Semester – Except Semester II)**  
**UG / PG (FT/PT) Degree Programmes**

Sl. No.	Programme	Semester	Commencement of Classes	Last working day		Commencement of Practical Examinations		Commencement of End Semester Examinations	
				Existing	Revised	Existing	Revised*	Existing	Revised*
1.	B.E. / B.Tech. (Full-Time)	IV,VI	06.02.2023	12.05.2023	24.05.2023**	15.05.2023	25.05.2023	26.05.2023	05.06.2023
2.	B.E. / B.Tech. (Full-Time)	VIII	06.02.2023	12.05.2023**	-	15.05.2023	-	26.05.2023	-
3.	B. Arch. (Full-Time)	IV,VI,VIII,X							
4.	B.E. / B.Tech. (Part-Time)	IV,VI							
5.	M.B.A. (Full-Time & Part-Time)	IV							
6.	M.B.A. (5 Yrs-Integrated)	IV,VI,VIII,X							

**RE - OPENING DAY FOR THE NEXT SEMESTER: 07.08.2023 (Monday)**

\* To provide additional classes for Skill Based Courses.

**NOTE:**

1. The Theory and Practical Examination schedules will be published in due course (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

\*\* In order to ensure minimum no. of working days, the following Saturdays are declared as working days.

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
1.	11.02.2023	Monday
2.	18.02.2023	Tuesday
3.	25.02.2023	Wednesday
4.	04.03.2023	Thursday
5.	11.03.2023	Friday
6.	18.03.2023	Monday

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
7.	25.03.2023	Tuesday
8.	01.04.2023	Wednesday
9.	29.04.2023	Thursday
10.	06.05.2023	Friday
11.	13.05.2023	Monday**
12.	20.05.2023	Tuesday**

*[Signature]*  
**PRINCIPAL**

**ANNA VELAYUTHI COLLEGE OF ENGINEERING**  
**POTTALKULAM**  
**AZHAGAPPARCOVE - 625 401**  
**KANNIYAKUMARI DIST.**

*[Signature]*  
**30/3/2023**

**DIRECTOR**  
**ACADEMIC COURSES**

DAC-88



Date: 27.08.2022

**REVISED**



**CENTRE FOR ACADEMIC COURSES**

**ANNA UNIVERSITY: : CHENNAI - 600 025**

**ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES**

**June 2022 - October 2022 (Even Semester - Semester II)**

**PG (FT) Degree Programmes**

Sl. No	Programme	Semester	Commencement of Classes	Last working day	Commencement of Practical Examinations	Commencement of End Semester Examinations	
						Existing	Revised
1.	M.E. / M. Tech. / M. Arch.(FT)	II	27.06.2022	30.09.2022**	06.10.2022	17.10.2022	26.10.2022

**RE-OPENING DAY FOR THE NEXT SEMESTER: 16.11.2022 (Wednesday)**

1. Theory and Practical Examination schedules will be published in due course. (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

\*\* In order to ensure minimum no. of working days, the following Saturdays are declared as working days.

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
1.	02.07.2022	Thursday
2.	16.07.2022	Tuesday
3.	30.07.2022	Friday
4.	13.08.2022	Monday
5.	27.08.2022	Tuesday

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
6.	03.09.2022	Wednesday
7.	10.09.2022	Thursday
8.	17.09.2022	Friday
9.	24.09.2022	Monday

  
**PRINCIPAL**  
**ANNA UNLAKSHMI COLLEGE OF ENGINEERING**  
**POTTALURAI**  
**AZHAGAPPURAM - 619 401**  
**KANYAKUMARI DIST.**

  
**DIRECTOR**  
**ACADEMIC COURSES**

DAC - 58

ANNA UNIVERSITY:: CHENNAI 600 025

Internal Assessment Schedule for Non Autonomous Affiliated Institutions

NOVEMBER 2022 – MARCH 2023 - (SEMESTER – I)

UG (FT) Degree Programmes

Report No	Report Period	Test Period	Report Entry Period
I	28-11-2022 – 24-01-2023	18-01-2023 – 24-01-2023	25-01-2023 – 03-02-2023
II	25-01-2023 – 23-03-2023	16-03-2023 – 23-03-2023	23-03-2023 – 25-03-2023

Saturdays may be included as working days to make good the Shortages, if any.

*P. Senthil*  
06.01.2023  
CONTROLLER OF EXAMINATIONS

*[Signature]*  
PRINCIPAL  
ANNA VALANSAMI COLLEGE OF ENGINEERING  
POTTAKULAM  
AZHAGAPPAPURAM - 625 451  
KANNIYAKUMARI DIST.

ANNA UNIVERSITY:: CHENNAI 600 025

Internal Assessment Schedule for Non Autonomous Affiliated Institutions

AUGUST 2022 – DECEMBER 2022 - (SEMESTER - III)

UG (IT&PT) & PG(M.B.A) (Syrs Integrated) Degree Programmes

Report No	Report Period	Test Period	Report Entry Period
I	22-08-2022 – 15-10-2022	10-10-2022 – 15-10-2022	15-10-2022 – 21-10-2022
II	17-10-2022 – 08-12-2022	02-12-2022 – 08-12-2022	08-12-2022 – 10-12-2022

Saturdays may be included as working days to make good the Shortages, if any.

*P. Senthil*  
19-09-2022  
CONTROLLER OF EXAMINATIONS

*[Signature]*  
PRINCIPAL  
ANNA WALAPPAI COLLEGE OF ENGINEERING  
KULAM  
ANNAMALAYUR  
KULAM - 625 001  
KULAM DIST.

**ANNA UNIVERSITY:: CHENNAI 600 025**

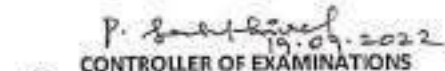
**Internal Assessment Schedule for Non Autonomous Affiliated Institutions**

**AUGUST 2022 - DECEMBER 2022 - For all UG - Programmes (ODD SEMESTER-EXCEPT III SEMESTER)**

Report No	Report Period	Test Period	Report Entry Period
I	10-08-2022 – 23-08-2022	----	29-09-2022 – 06-10-2022
II	24-08-2022 – 21-09-2022	16-09-2022 – 21-09-2022	29-09-2022 – 06-10-2022
III	22-09-2022 – 21-10-2022	17-10-2022 – 21-10-2022	21-10-2022 – 29-10-2022
IV	22-10-2022 – 19-11-2022	14-11-2022 – 19-11-2022	19-11-2022 – 21-11-2022

Saturdays may be included as working days to make good the Shortages, if any.

  
PRINCIPAL  
ANNA UNIVERSITY COLLEGE OF ENGINEERING  
POTTALIVILAM  
AZHAGAPPAPURAM - 609 401  
KANNIYAKUMARI DIST.

  
19.09.2022  
CONTROLLER OF EXAMINATIONS

ANNA UNIVERSITY:: CHENNAI 600 025

Internal Assessment Schedule for Non Autonomous Affiliated Institutions

OCTOBER 2022 – JANUARY 2023 - (SEMESTER – I)

PG (FT&PT) Degree Programmes - M.B.A&M.BA(INTEGRATED)

Report No	Report Period	Test Period	Report Entry Period
I	10-10-2022 – 02-12-2022	28-11-2022 – 02-12-2022	19-12-2022 – 23-12-2022
II	03-12-2022 – 25-01-2023	20-01-2023 – 25-01-2023	25-01-2023 – 27-01-2023

Saturdays may be included as working days to make good the Shortages, if any.



PRINCIPAL  
ANNA VALAMANGI COLLEGE OF ENGINEERING  
POTTALICULAM  
AZHAGAPPAPURAM - 629 601  
KANNIYAKUMARI DIST.

*(Signature)*

*P. Senthil*  
19-12-2022  
19.12.2022  
CONTROLLER OF EXAMINATIONS

ANNA UNIVERSITY:: CHENNAI 600 025

Internal Assessment Schedule for Non Autonomous Affiliated Institutions

DECEMBER 2022 – MARCH 2023 - (SEMESTER – III)

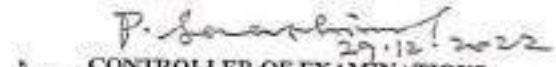
PG (FT) Degree Programmes - M.E. / M.Tech. / M.Arch.

Report No	Report Period	Test Period	Report Entry Period
I	12-12-2022 – 01-02-2023	27-01-2023 – 01-02-2023	01-02-2023 – 07-02-2023
II	02-02-2023 – 23-03-2023	17-03-2023 – 23-03-2023	23-03-2023 – 25-03-2023

Saturdays may be included as working days to make good the Shortages, if any.



PRINCIPAL  
ANNA WALAISANGH COLLEGE OF ENGINEERING  
POTTALKULAM  
AZHAGAPPAPURAM - 623 401  
KANNIYAKUMARI DIST.



29.12.2022  
CONTROLLER OF EXAMINATIONS

**ANNA UNIVERSITY:: CHENNAI 600 025**

**Internal Assessment Schedule for Non Autonomous Affiliated Institutions**

**April 2022 – July 2022 - (SEMESTER - II)**

**B.E./B.TECH.(FT/PT) Degree Programmes & M.B.A. (FT/PT/5 Yrs - Integrated) Degree Programmes**


Report No	Report Period	Test Period
I	04-04-2022 – 21-05-2022	16-05-2022 – 21-05-2022
II	23-05-2022 – 04-07-2022	28-06-2022 – 04-07-2022

**April 2022 – July 2022 - (SEMESTER - II)**


**B.ARCH.(FT) Degree Programme**

Report No	Report Period	Test Period
I	04-04-2022 – 06-05-2022	29-04-2022 – 06-05-2022
II	07-05-2022 – 04-06-2022	30-05-2022 – 04-06-2022
III	06-06-2022 – 04-07-2022	28-06-2022 – 04-07-2022

Saturdays may be included as working days to make good the Shortages, if any.

  
PRINCIPAL  
ANNA TALARAJU COLLEGE OF ENGINEERING  
POTTALKULAM  
ACHANAPALLE ROAD - 600 101  
KANNIYAKUMARI DIST.

  
09/05/2022

  
09.05.2022

  
20.05.2022  
CONTROLLER OF EXAMINATIONS (J/c)

ANNA UNIVERSITY:: CHENNAI 600 025  
OFFICE OF THE CONTROLLER OF EXAMINATION

February 2023 – May 2023 - (SEMESTER - IV) – R-2023  
FOR ALL UG (PG/MBA) PROGRAMMES

Report No	Report Period	Test Period	Report Entry Period
I	06-03-2023 – 21-03-2023	15-03-2023 – 21-03-2023	21-03-2023 – 26-03-2023
II	23-03-2023 – 12-05-2023	08-05-2023 – 12-05-2023	12-05-2023 – 15-05-2023

Saturdays may be included as working days to make good the Shortages, if any.

*P. Senthil Kumar*  
13.03.2023  
CONTROLLER OF EXAMINATIONS

*13/03/2023*

*As*  
13-03-23

*Ahmed*  
PRINCIPAL  
ANNA UNIVERSITY COLLEGE OF ENGINEERING  
POH TALUKKURAI  
AZHAKKOTTAI - 600 001  
KANNIYAKUMARI DISTRICT



**ANNA UNIVERSITY :: CHENNAI 600 025**

**Internal Assessment Schedule for Non Autonomous Affiliated Institutions**

**MARCH - JUNE 2022 - For all UG - Programmes (Even Semester - Except Semester II)**

Report No	Report Period	Test Period	Report Entry Period
I	16-03-2022 - 01-04-2022	---	21-04-2022 - 25-04-2022
II	04-04-2022 - 29-04-2022	25-04-2022 - 29-04-2022	29-04-2022 - 04-05-2022
III	30-04-2022 - 24-05-2022	19-05-2022 - 24-05-2022	24-05-2022 - 28-05-2022
IV	25-05-2022 - 18-06-2022	11-06-2022 - 16-06-2022	16-06-2022 - 17-06-2022

Saturdays may be included as working days to make good the Shortages, if any.

  
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20.06.2022  
CONTROLLER OF EXAMINATIONS I  
  




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Website: [www.avce.edu.in](http://www.avce.edu.in)

EXAM CELL

DATE: 10-03-2023

CIRCULAR

All faculty members are hereby informed that Internal Assessment Test-I will be held from 15-03-2023 to 20-03-2023

Exam Cell

Principal

Copy To:

- The Chairman
- The Director
- Vice-Principal
- All HODs



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**ANNA VAILANKANNI COLLEGE OF ENGINEERING**  
 AVK Nagar, Pottalkulam, Azhagappapuram P.O, Kanyakumari District -629 401  
**ACADEMIC YEAR 2022-2023(EVEN)**  
**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**  
**INTERNAL ASSESSMENT TEST - I**  
**TIME TABLE**

DATE	TIME	ECE		
		II YEAR	III YEAR	IV YEAR
15/03/2023	2.00 TO 3.30PM	EC3452 - Electromagnetic Fields	EC8691 – Microprocessors and Microcontrollers	GE8076 – Professional Ethics in Engineering
16/03/2023	2.00 TO 3.30PM	EC3401 - Networks and Security	EC8652 – Wireless Communication	EC8094 – Satellite Communication
18/03/2023	11.00 TO 12.30PM	EC3451 - Linear Integrated Circuits	MG8591 – Principles of management	-
	2.00 TO 3.30PM	EC3492 - Digital Signal Processing	EC8651 – Transmission Lines and RF Systems	-
20/03/2023	11.00 TO 12.30PM	EC3491 - Communication Systems	EC8095 – VLSI Design	-
	2.00 TO 3.30PM	GE3451 - Environmental Sciences and Sustainability	EC8002 – Multimedia Compression and Communication	-

*S. Praveen*  
IT Coordinator



*P. Ananya*  
HOD  
*A. Anjali*  
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*S. Anjali*  
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ACADEMIC YEAR 2022-2023(EVEN)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING  
 INTERNAL ASSESSMENT TEST - 2  
 TIME TABLE

DATE	TIME	ECE		
		II YEAR	III YEAR	IV YEAR
17/04/2023	11.00 TO 12.30PM	EC3452 - Electromagnetic Fields	MG8591 - Principles of Management	-
	2.00 TO 3.30PM	EC3401 - Networks and Security	EC8095 - VLSI Design	EC8094 - Satellite Communication
18/04/2023	11.00 TO 12.30PM	EC3451 - Linear Integrated Circuits	EC8691 - Microprocessors and Microcontrollers	-
	2.00 TO 3.30PM	EC3492 - Digital Signal Processing	EC8651 - Transmission Lines and RF Systems	GE8076 - Professional Ethics in Engineering
19/04/2023	11.00 TO 12.30PM	EC3491 - Communication Systems	EC8002 - Multimedia Compression and Communication	-
	2.00 TO 3.30PM	GE3451 - Environmental Sciences and Sustainability	EC8652 - Wireless Communication	-

*S. Princy*  
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*Danya*  
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*J. S. Srinivasan*  
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ACADEMIC YEAR 2022-2023(EVEN)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING  
 MODEL EXAMINATION  
 TIME TABLE

DATE	TIME	ECE		
		II YEAR	III YEAR	IV YEAR
15/05/2023	12.30 TO 03.30PM	EC3452 - Electromagnetic Fields	MG8591 – Principles of Management	-
16/05/2023	12.30 TO 03.30PM	EC3401 - Networks and Security	EC8095 – VLSI Design	EC8094 – Satellite Communication
17/05/2023	12.30 TO 03.30PM	EC3451 - Linear Integrated Circuits	EC8691 – Microprocessors and Microcontrollers	-
18/05/2023	12.30 TO 03.30PM	EC3492 - Digital Signal Processing	EC8651 – Transmission Lines and RF Systems	GE8076 – Professional Ethics in Engineering
19/05/2023	12.30 TO 03.30PM	EC3491 - Communication Systems	EC8002 – Multimedia Compression and Communication	-
22/05/2023	12.30 TO 03.30PM	GE3451 - Environmental Sciences and Sustainability	EC8652 – Wireless Communication	-

*S. Princy*  
 TICoordinator



*Denya*  
 HOD

*Abdeli*  
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*J. J. J.*  
 PRINCIPAL

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING INTERNAL TEST-I

Subject Code/ Subject Name: EC8691 Microprocessors and Microcontrollers

Year/Branch : III ECE

Time: 2.00-3.30 PM

Date: 15/3/2023

### Part: A (5\*2=10)


Q.No	COs	Cognitive Level	Questions
1	CO1	K1	Draw the format of 8086 flag register
2	CO1	K1	What is linker?
3	CO1	K1	Calculate the physical address, when segment address is 1085H and effective address is 4537H.
4	CO2	K2	What is the operation of S0, S1 and S2 pins in maximum mode?
5	CO2	K4	In an 8086 microprocessor, the contents of the accumulator and the carry flag are A7 (in hex) and 0, respectively. If the instruction RLC is executed, then the contents of the accumulator (in hex) and the carry flag, respectively, will be----- (GATE-2016)

### Part: B (2\*16=32)

Q.No	COs	Cognitive Level	Questions
6(a)	CO1	K3	Explain the data transfer group and logical group of 8086 instructions
			OR
6(b)	CO1	K2	Explain the internal hardware architecture of 8086 microprocessor with neat diagram
7(a)	CO2	K3	Draw and explain the minimum mode of 8086
			OR
7(b)	CO2	K3	Explain closely coupled and loosely coupled configuration

### Part: C (1\*8=8)

Q.No	COs	Cognitive Level	Questions
8 (a)	CO1	K3	Explain different types of interrupts in 8086
			OR
8 (b)	CO2	K3	Write about coprocessor configuration

  
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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING INTERNAL TEST-II

Subject Code/ Subject Name: EC8691 Microprocessors and Microcontrollers

Year/Branch : III ECE

Time: 11.00-12.30 PM

Date: 18/3/2023

### Part: A(5\*2=10)


Q.No	COs	Cognitive Level	Questions
1	CO3	K1	Mention the features of 8251 Serial Communication Interface
2	CO3	K1	Differentiate memory mapped I/O and I/O mapped I/O
3	CO4	K1	Write an ALP in 8051 to multiply the given number 55h and 87h. [Gate 2016]
4	CO4	K2	Write about BIT manipulation instructions of 8051.
5	CO4	K4	Write a program to add two 16 bit nos in 8051. The numbers are 4590 and 1234 . Store the sum in R7 and R6.

### Part: B(2\*16=32)

Q.No	COs	Cognitive Level	Questions
6(a)	CO3	K3	Explain in detail about serial communication interface-8251 with neat block diagram
			OR
6(b)	CO3	K3	Draw the functional block diagram of 8254 programmable interval timer and explain the different modes of operation.
7(a)	CO4	K3	With neat diagram explain the architecture of 8051 microcontroller
			OR
7(b)	CO4	K3	(i) Memory organization of 8051 (ii) Port P0 and P1 circuits

### Part: C(1\*8=8)

Q.No	COs	Cognitive Level	Questions
8 (a)	CO3	K3	Describe Traffic light controller interfacing .also write the program code.
			OR
8 (b)	CO4	K3	Illustrate the different addressing modes of 8051

  
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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING MODEL EXAMINATION

Subject Code: EC8551

Subject Name: COMMUNICATION NETWORKS

Time

Year/Branch :III/6

### Part: A(5\*2=10)

Q.No	COs	Cognitive Level	Questions
1	CO1	K1	Draw the flag register format of 8086 ?
2	CO1	K2	Calculate the physical address, when segment address is 1085 H and effective address is 4537 H.
3	CO2	K1	List the advanced microprocessors.
4	CO2	K1	What is main programming ?
5	CO3	K3	In an 8686 microprocessor, the contents of the accumulator and the carry flag are A7 (in hex) and 0, respectively . If the instruction RLC is executed ,then the contents of the accumulator (in hex) and the carry flag, respectively will be--- ---(GATE-2016)
6	CO3	K1	List the four display modes of 8279 keyboard/ display controller
7	CO4	K1	Give the alternate function for the port pins of port 3?
8	CO4	K1	Name the special functions registers available in 8051?
9	CO5	K1	Which register is used for serial programming in 8051? Illustrate it.
10	CO5	K2	Which register is used for serial programming in 8056? Illustrate it

### Part: B(5X13=65)

Q.No	COs	Cognitive Level	Questions
11(a)	CO1	K2	Explain the internal hardware architecture of 8086 microprocessor with neat diagram
			OR
11(b)	CO1	K2	Discuss the interrupts types of 8086 microprocessor?
12(a)	CO2	K3	Explain closely coupled and loosely coupled configuration?
			(or)
12(b)	CO3	K2	Draw and explain the minimum mode of 8086?



13(a)	CO3	K2	Explain D/A and A/D interfacing done with 8086 with an application.
			OR
13(b)	CO3	K2	Draw the functional block diagram of 8254 timer and explain the different modes of operation
14(a)	CO4	K2	Explain the memory organization of 8051 microcontroller.
			OR
14(b)	CO4	K2	Draw the pin diagram of 8051 microcontroller and explain the function of pin.
15(a)	CO5	K2	Describe the difference modes of operation of timers/counters in 8051 with its associated register.
			OR
15(b)	CO5	K3	Draw the diagram to interface a stepper motor with 8051 microcontroller and explain. Write a 8051 assembly language program to run and the stepper motor in both forward and reverse direction with delay

**Part: C(15X1=15)**

Q.No	COs	Cognitive Level	Questions
16(a)	CO3	K3	Explain with neat block diagram the working of parallel communication interfacing chip.
			OR
16(b)	CO1	K4	(i) Write the assembly language program to transfer a block of data between memory locations. (ii) Write the assembly language program for counting the number of 1's in a register



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Permanent Affiliation for B.E. - Computer Science Engineering

Pottalkulam, Pothalyadi Salai, Azhagappapuram Post, K.K. Dist. - 629 401.

Date: 15/12/22

Name: V. Ganga Roll No.: 20RE102 Branch: ECE  
Year / Semester: III year Subject Code / Title: EC2691 Microprocessors and microcontroller  
Name of the Examination: Internal Exam I/II/III Total No. of Pages:

6(b)

Architecture of 8086 :-

Part - B

42  
50

84  
9009

The 8086 CPU is divided into two independent functional ports.

1. Bus interface unit (BIU)
2. Execution unit (EU)

\* The BIU interface the 8086 to the outside world. The BIU fetches read data from memory and ports and write data to memory and I/O ports.

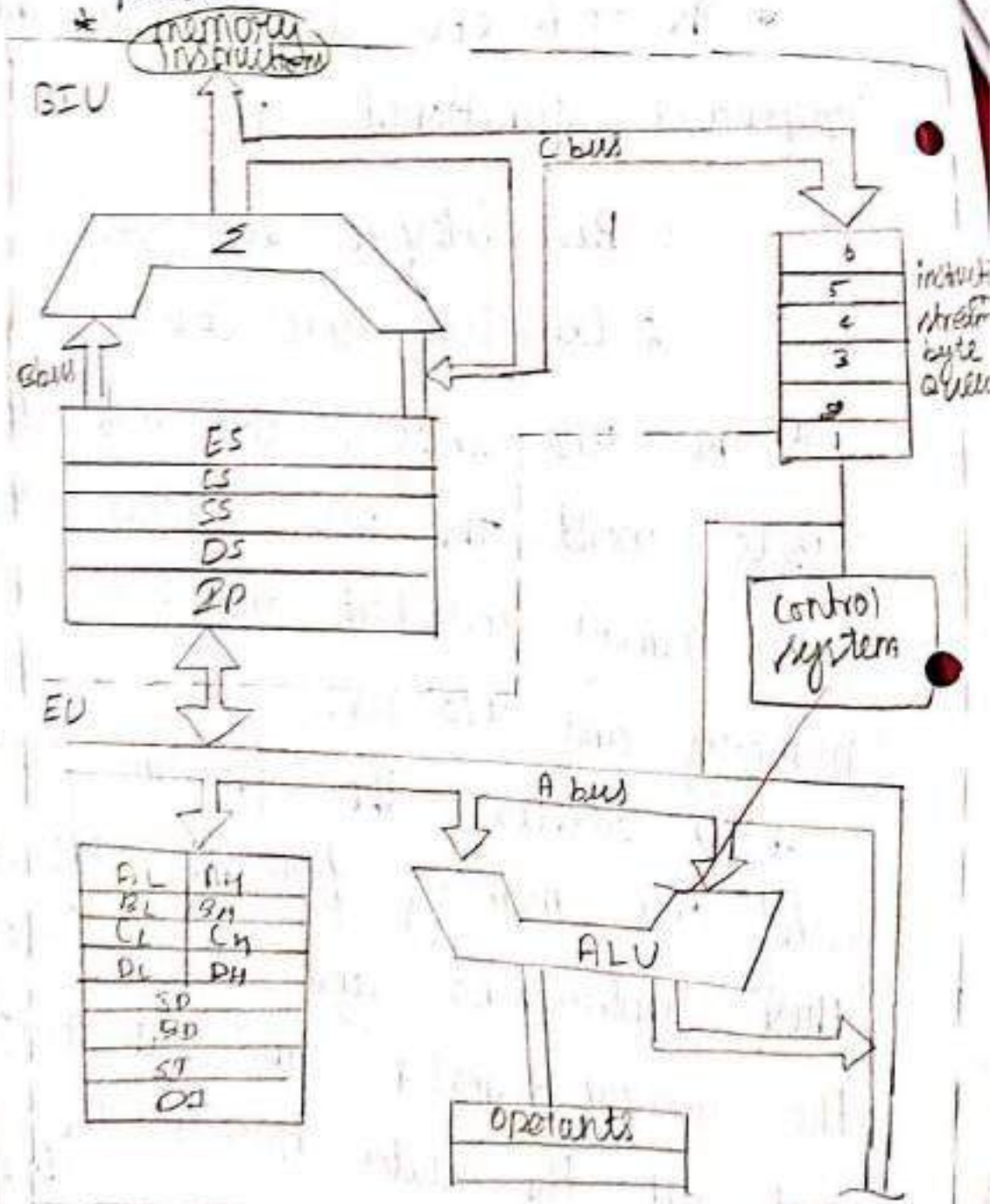
\* EU receives the program instruction code and memory from the BIU, executes these instructions and the results stored the general registers and the output put all the data through the BIU.

BIU contain -

- \* segment register
- \* instruction pointer
- \* instruction Queue

EU contain -

- \* ALU
- \* general purpose registers
- \* index registers
- \* pointers



## General Registers :-

\* The general purpose registers are,

1. Accumulator register (AX)
2. Base register (BX)
3. Count register (CX)
4. Data register (DX).

### 1. Accumulator Register (AX) :-

\* Accumulator register is the 16 bit register also divided into two 8 bit registers AL and AH.

\* AL contain lower order byte and AH contain higher order byte.

\* Accumulator can be used for I/O operation and string manipulation.

### 2. Base Register (BX) :-

\* Base register is a 16 bit register also contain two 8 bit registers BL and BH.

\* BL contain lower order byte and BH contain higher order byte.

\* BL can contain a data byte used for Based,  $B_{ind}$  indexed and register indirect addressing.

### 3. Count register (CX) :-

- \* Count register is a 16 bit register.
- Contain two 8-bit registers CL and CH.
- \* CL contain lower order byte and CH contain higher order byte.
- \* CL can contain string manipulation and shift/rotate registers.

### 4. Data register (DX) :-

- \* Data register is a 16 bit register also contain two 8 bit registers DL and DH.
- \* DL contain lower order bytes DH contain higher order byte.
- \* DL can be used as an numbers in the I/O operation.

### Segment registers :-

- \* The segment registers are,

  1. code segment (CS)
  2. stack segment (SS)
  3. data segment (DS)
  4. extra segment (ES)

1. Code segment:-

\* Code segment is a 16 bit register contain address 64KB segment with program instruction.

\* Code segment cannot be changed directly.

2. Stack segment:-

\* Stack segment is a 16 bit register contain address 64KB segment with program Stack.

\* By default the processor assume that the all data instructions referenced by stack pointer and Base pointer registers located at the stack segment.

\* Stack segment can be changed directly using pop instructions.

3. Data segment:-

\* Data segment is a 16 bit register contain address 64KB segment with program data.

By default the processor assume that the all data referenced by general registers and index registers located at

the data segment.

\* data segment can be changed directly using pop and LDS instructions.

4. Extra segment:-

\* Extra segment is a 16 bit register.

\* ES can be changed directly using pop and LES instructions.

Pointers:-

Stack pointer:-

\* Stack pointer is a 16 bit register pointing to program stack

~~data~~ Base pointer:-

\* BP is a 16 bit register pointing to data the program stack

Index registers:-

Source indexed (SI):-

\* SI is a 16 bit register

\* DI is used for based, based indexed as well as source data address string manipulation.

destination indexed (DI): -

- \* DI is a 16 bit register
- \* EI is used for based, based indexed as well as destination data address string manipulation.

Instruction pointer (IP): -

- \* IP is the 16 bit register.
- \* The operation same as the program counter.

Flags: -

- \* Flags is the 16 bit register also contain nine 1 bit flags.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				DF	DF	IF	TF	SF	ZF		AF		PF		CF

Conditional flags: - OF, SF, ZF, PF, AF, CF

Control flags: - DF, IF, TF

OF :- Overflow flag (-) :-

- \* It is set if there overflow occurs

SF :- Sign Flag.

- \* It is set if the most significant bit of the result is set.



Zero flag :-

\* If the set there is no res (0)

Trap flag :-

\* If the set, the trap executes

after every instruction

Instruction Queue :-

\* The Instruction Queue is the first in first out (FIFO) group of registers where the 6 bits instruction code is from memory.

Arithmetic and Logic Unit :-

\* It is a 16 bit register. It can add, subtract, increment, decrement and perform AND, OR, NOT, XOR

1(a)

## Minimum mode configuration:-

- \* Minimum mode pin 33 - master clock
- \* All the control signals are given out the microprocessor chip itself
- \* There is only single microprocessor in the minimum mode configuration.
- \* The system components are, latches, Transceivers, clock generator, memory, I/O devices.
- \* Latches are generally a D Flip Flop like PC8229.
- \* They are used for separation of valid address from multiplexed address data signal.
- \* Latches are controlled by FILE.
- \* Three latches are used for 20 address lines.
- \* Transceivers is a bidirectional buffers.

\* Transceivers are used for <sup>separate</sup> data from the time multiplexed data signals.

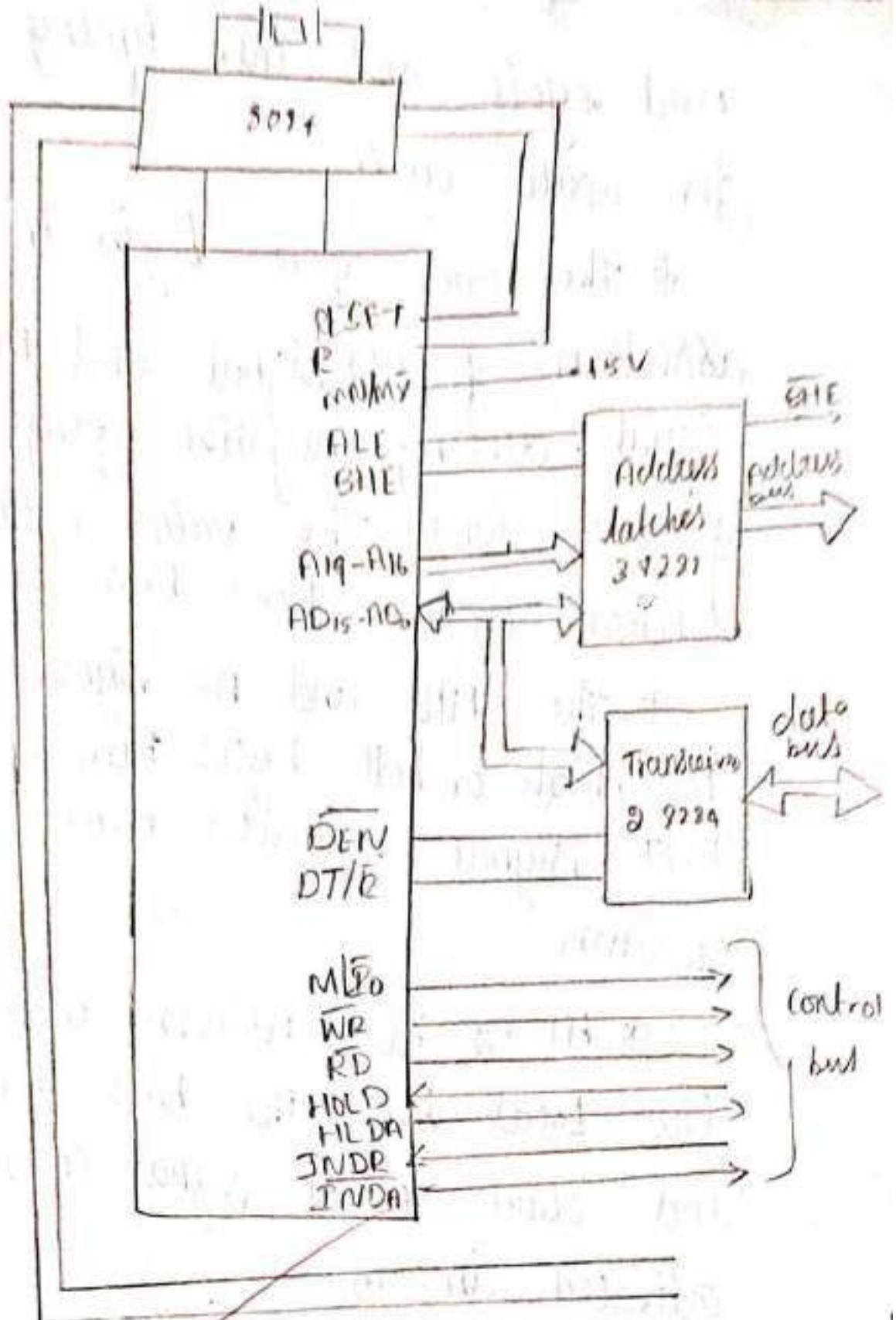
\* They are controlled by DEN and  $\overline{PT/\overline{R}}$ .

\* Memory contain monitor & user program storage.

\* EEPROM used for monitor storage

\* RAM used for user program storage.

\* clock generator are generates the clock from the crystal oscillator. Then ~~it~~ shape it and make to its more precision. they are used for accurate timing referenced in the minimum mode.



Bus timing for minimum mode :-

\* The opcode fetch and Read cycle are similar. Hence the timing diagram can be categorized into two parts.

The first part is timing diagram for

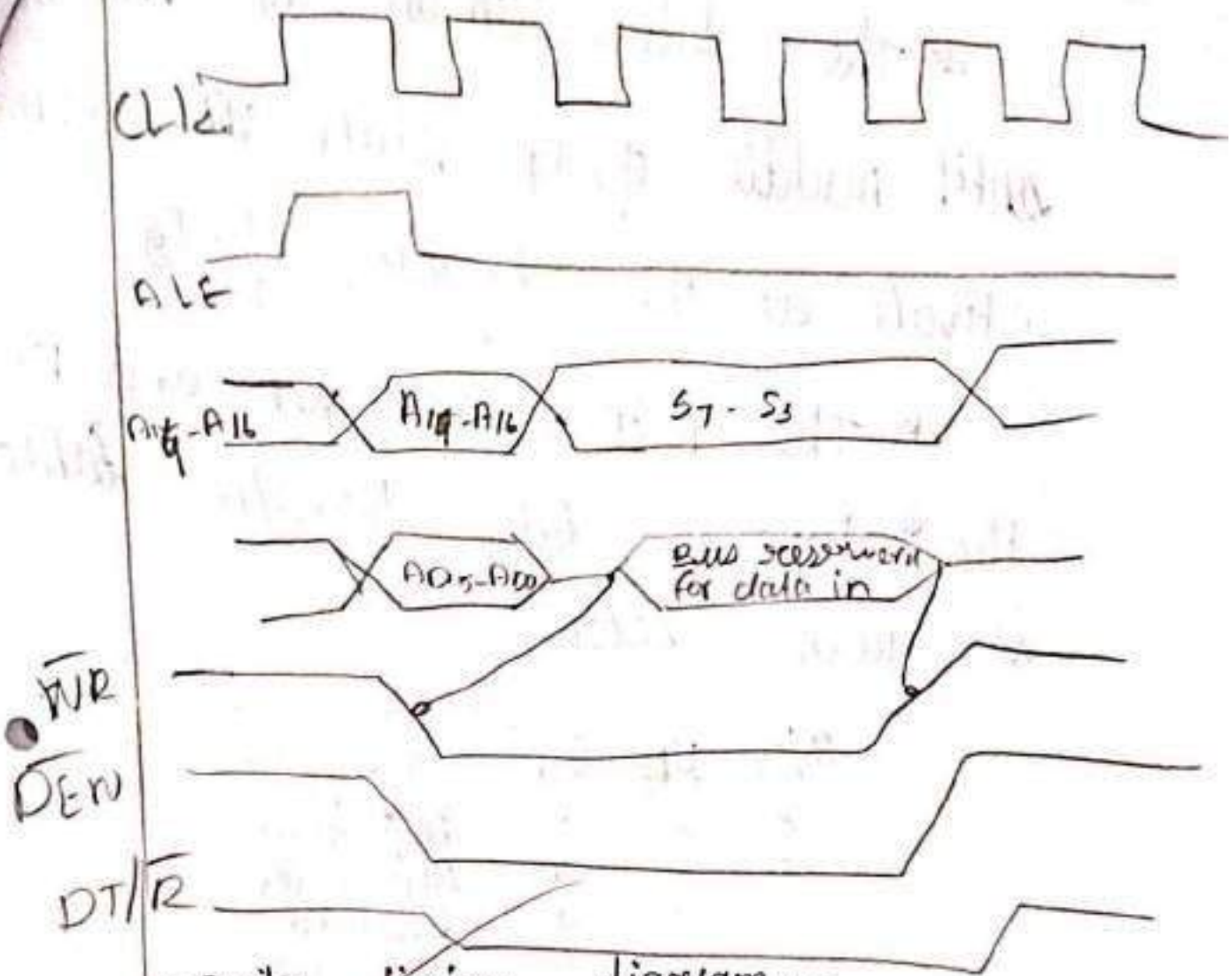
read cycle and other timing details for write cycle.

\* The read cycle begins in  $T_1$  with assertion of (ALE) signal and M/IO signal. During negative going edge of this signal, the valid address latched on the local bus.

\* The BHE and A<sub>0</sub> signals Address low, high or both bytes. From  $T_1$  to  $T_4$  the M/IO signal indicates memory or I/O operation.

\* At  $T_2$ , the Address removed from the local bus, the bus then tristates and read control signal (RD) also activated in  $T_2$ .

\* The Read signal causes the Addressed device to enable its data bus drivers. At RD goes low the <sup>valid</sup> data is available on the data bus.



write timing diagram :-

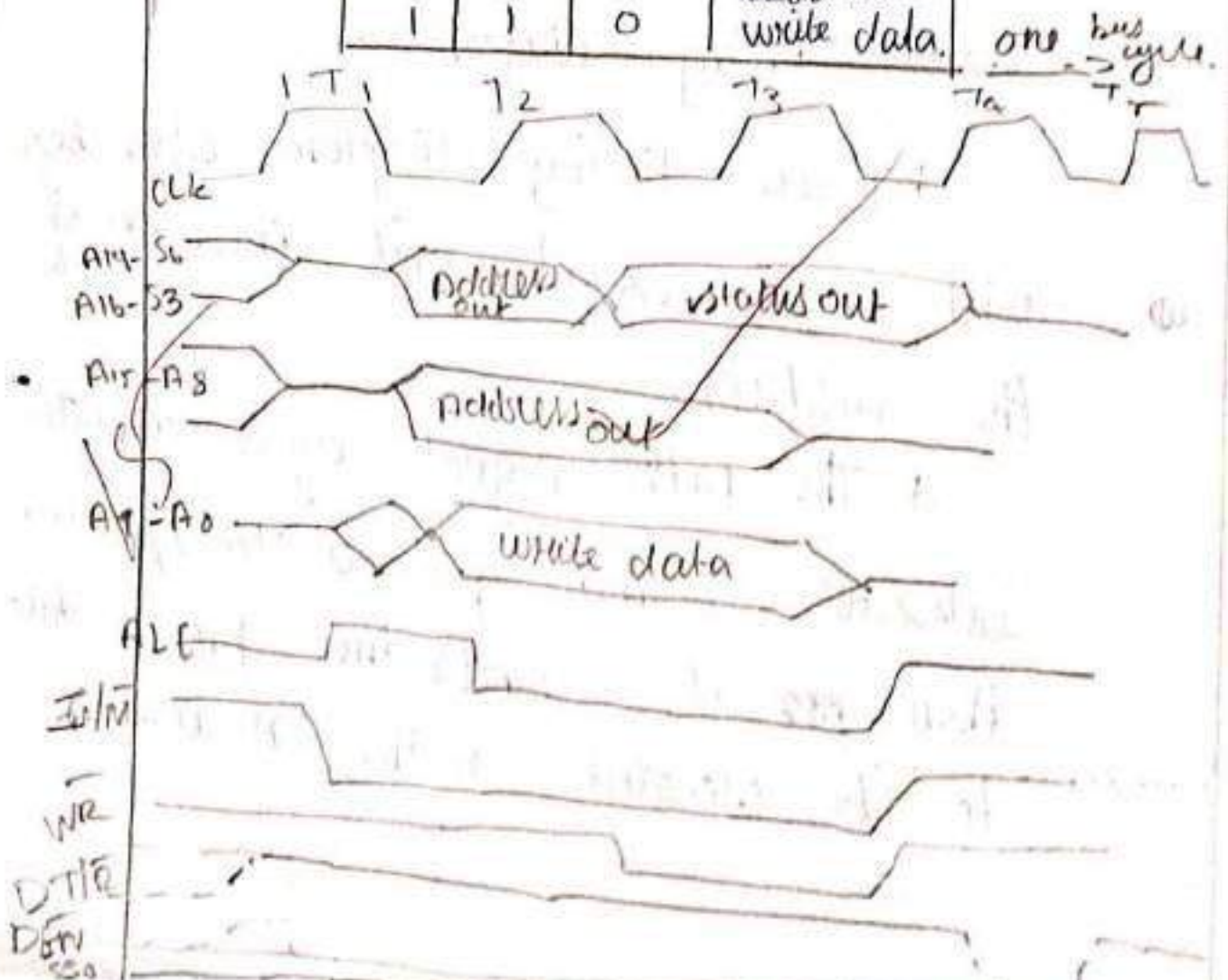
\* write timing diagram also begins with ALE signal and emission of the address.

\* The M/P<sub>0</sub> signal again asserted indicates a memory and I/O operation then ~~for~~ it sends the process data to be located on the Address.

\* The data remain on the bus until middle of  $T_4$  state.  $\overline{WR}$  become active at the beginning of  $T_3$ .

\* The M/P<sub>0</sub> and  $\overline{WR}$  and  $\overline{RD}$  the type of data transfer table is given below.

M/P <sub>0</sub>	$\overline{RD}$	$\overline{WR}$	Transfer type
0	0	1	M/P <sub>0</sub> read
0	1	0	M/P <sub>0</sub> write
1	0	1	Read data
1	1	0	write data.



Part: c.

8(b)

co processor configuration:-

\* The co processor and closely coupled configuration are similar to both the CPU and the external processor.

shares :-

\* memory

\* I/O system

\* clock generator

\* BUS and BUS control logic.

\* WAIT instruction allows the processor to be synchronized itself.

\* TEST input is asserted (low) when wait state is completed and executes then resume.

\* ESC instruction :- ESC opcode, operand.



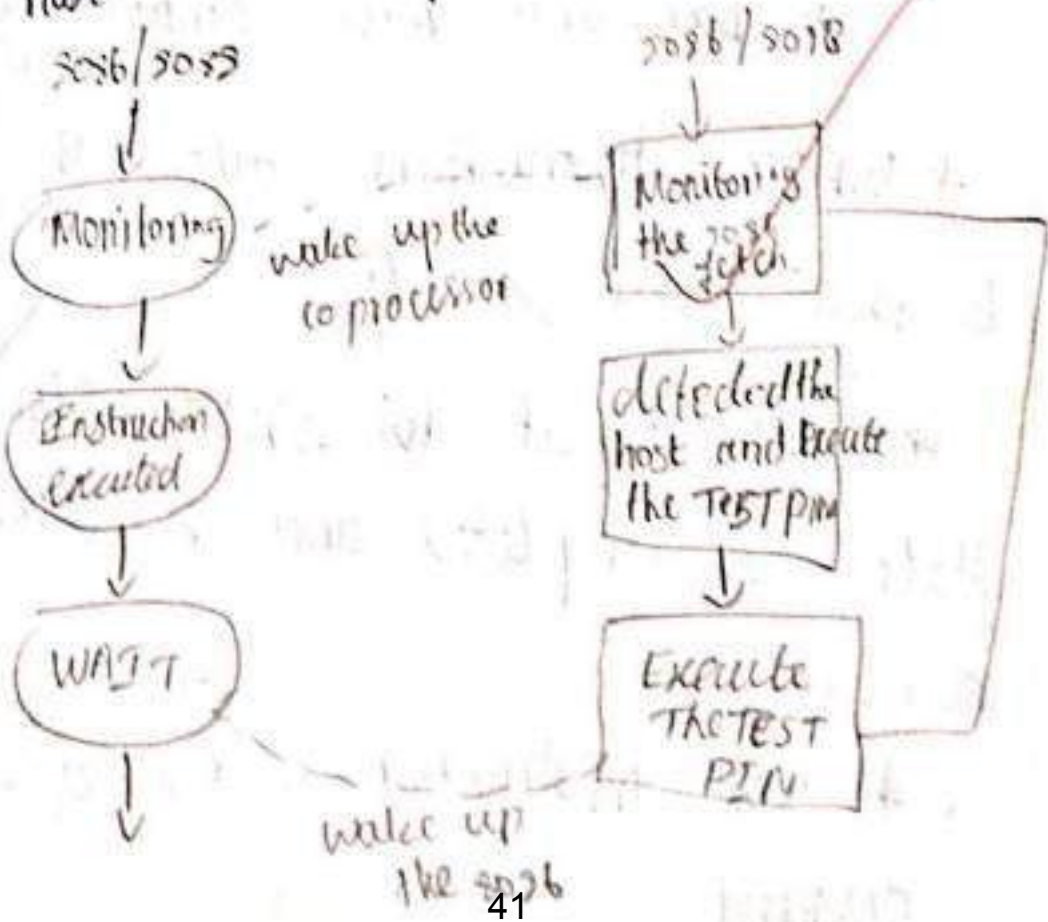
\* The co processor ~~does not~~ cannot take by the control signals. it does everything through the CPU.

\* The host shares CPU and clock and bus control logic

\* The communication with the host CPU by the way of shared.

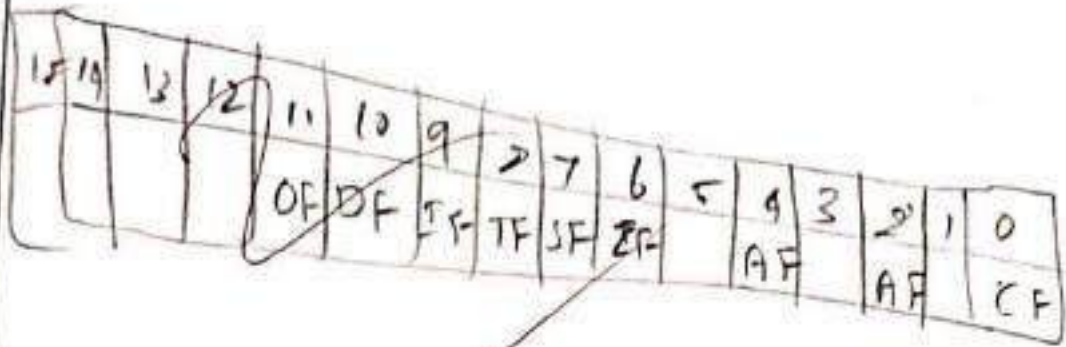
\* The host set up the message in monitor.

\* The independent host intercept host on completed.



Part: A.

1.



2.

3.

Physical address = segment address  $\times$  10H  
 + effective address.

$$= 1085H \times 10H + 4537H$$

$$= 10850 + 4537H$$

Physical address = ~~58287H~~ 15287H  
 (20bits).

5.

Content of the accumulator and the carry flag will be 4 and 1.

EC 869: microprocessor and  
microcontrollers

V. Ganga  
III Year

ECE

20RE108

Part: B

54

100

11)  
A)

Architecture of 8086:-

\* The 8086 CPU is divided into two independent functional parts -

Bus interface unit (BIU)  
execution unit (EU)

\* The 8086 the BIU interface is outside to the world. The BIU fetches read data from memory (or) ports and write data from to memory (or) ports.

\* The EU receives program instruction code to the BIU memory and its executes! and stored in the output them put all of its BIU.

BIU :-

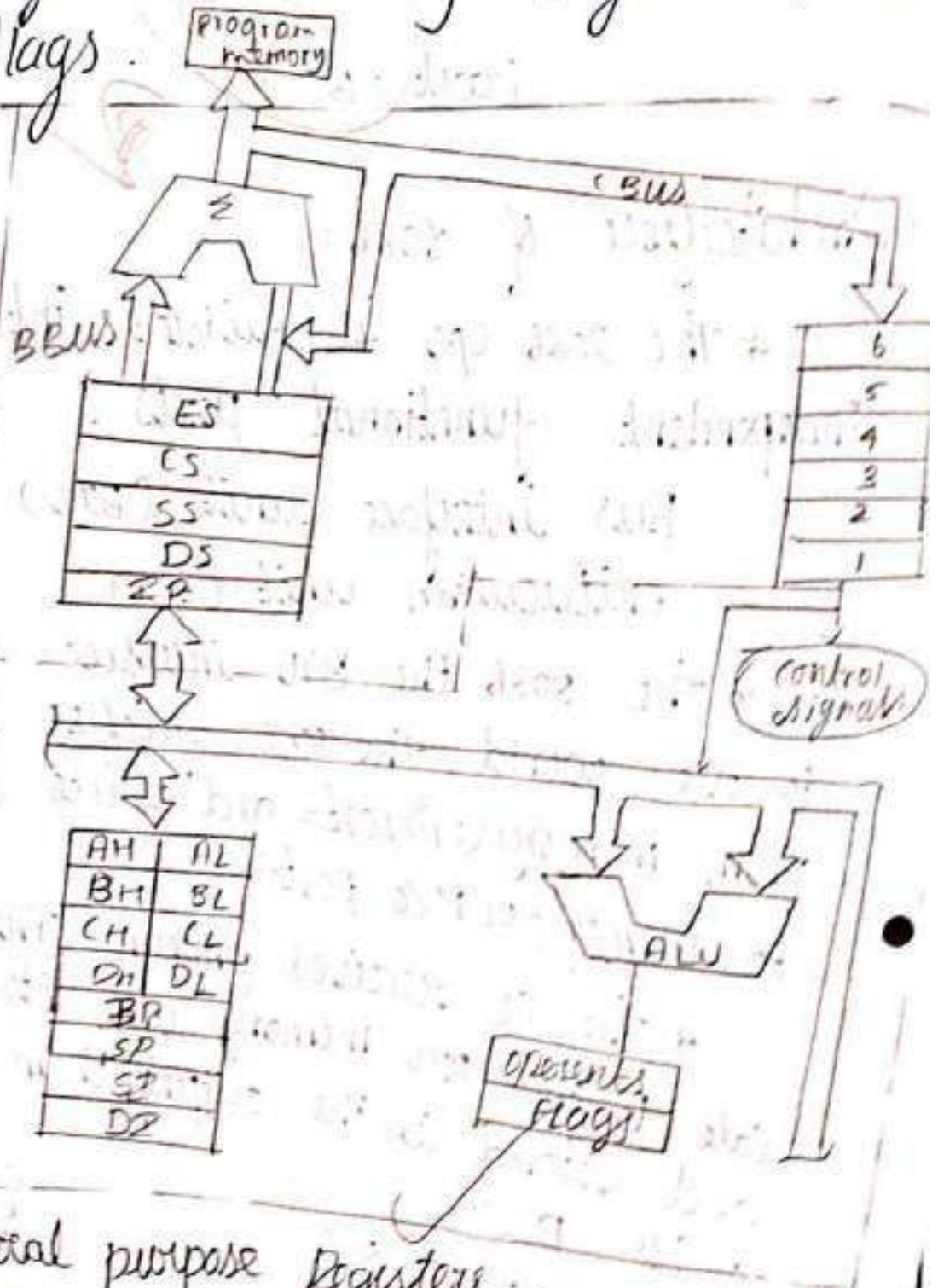
\* BIU contains stack segment (SS)

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# Instruction pointer, Instruction

EU :-

\* EU contains ALU, general purpose registers, Indexing registers, pointer flags.



General purpose Registers :-

The 16 bit general purpose registers are, AX, BX, CX, DX

## Accumulator Register (AX): -

\* It is a 16 bit register, consists of two 8 bit registers AL and AH.

\* AL consists of low order byte of the word and AH contains high order byte.

\* It is used for string manipulation.

## Base Register (BX): -

\* It is a 16 bit register, consists of two 8 bit registers BL & BH.

\* BH contains low order byte of the word and BL contains high order byte.

\* It is used for base, base indexed registers.

## Count Register (CX): -

\* It is a 16 bit register, consists of two 8 bit registers CL & CH.

\* CL contains low order byte of the word & CH contains high order byte.

\* It is used for counter in shift /

## Rotate Register

## Data Register (DX): -

\* It is a 16 bit register, consists of two 8 bit registers DL & DH.

\* DL contain low order byte & DI high order byte.

### Segments

- \* Extra segment
- \* Code segment
- \* Data segment
- \* Stack segment

### Code segment :-

\* 16 bit register contain address of 64KB segment. with processor instruction directly.

\* CS register cannot be changed

### Stack segment :-

\* 16 bit register contain address of 64KB segment with program stack

\* Stack segment register can be changed directly using pop instructions

### Data segment :-

\* 16 bit register contain address of 64 KB segment with program data.

\* Data segment can be changed directly using pop & LDS instructions.

Extra segment (ES): -

\* 16 bit register contains address of  $64K$  segment with program data.

\* ES can be changed directly using pop & LES instructions.

Pointers: -

Base pointers: -

\* 16 bit register pointing to data from the stack segment.

Stack pointers: -

\* 16 registers pointing to the stack segment.

Source Instruction: - (SP)

\* SP is a 16 bit register.

\* SP is used for base, base indexed register as well as source to the memory.

Destination Instruction: - (DP)

\* DP is a 16 bit register.

\* DP is used for index addressing.

base & base index registers as  
Destination to the source.

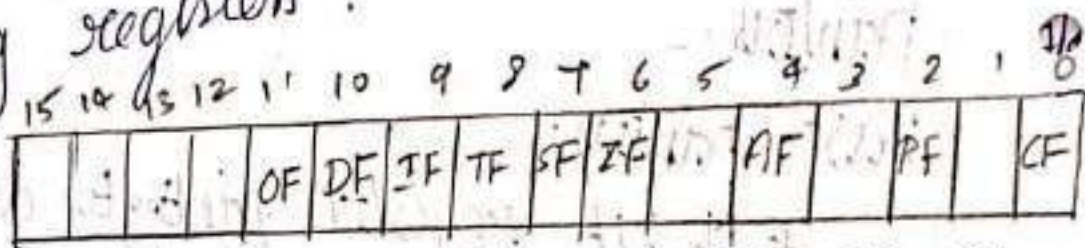
Instruction pointer:-

- \* IP is a 16 bit register
- \* IP operates like a program counter.

Flag Register:-

\* FR is a 16 bit register and nine bits

flag register



\* Condition flags:- DF, SF, ZF, AF, PF, CF

\* Control flags:- DF, IF, TF.

overflow flag (OF):- IP is set if an overflow occurs

sign flag (SF):- IP is set if an most significant bit as the result.

zero flag (ZF):- IP is set if the result is zero

Auxiliary carry flag (AF):- IP is used for BCD arithmetic.

Parity flag (PF):- IP is set if the most of significant bit as the last result.



Carry flag (CF) :- It is set the carry or borrow occurs.

Direction flag :- It is used for ALU.

Trap flag :- It is set a trap is executed every cycle.

Internal bus flag :- It is set control the registers.

Instruction Queue :-  
\* Instruction Queue is first in first out (FIFO) group of registers where 6 bytes of instruction code is prefixed the memory.

\* If the queue is full, the BPU does not perform any bus cycle.

ALU :-

\* It is 16 bit register used to perform arithmetic and logical operations such as add, subtract, divide, multiply and AND, OR, XOR operations.

✓

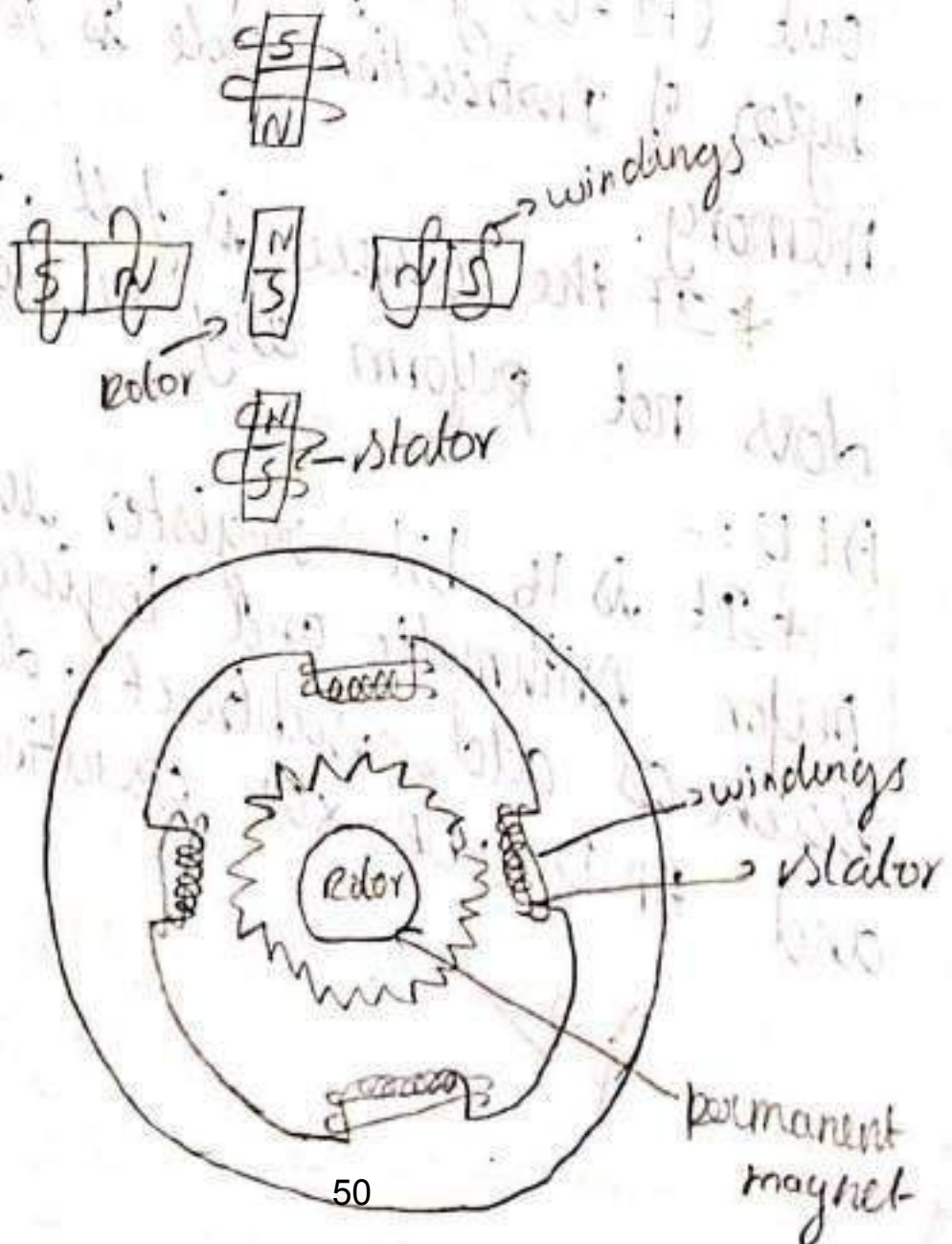
15)

## B) Stepper motor :-

\* stepper motor is a widely used device that translates electrical energy into mechanical movement.

\* stepper motor is used to applications such as, disk drives, dot matrix printers, robotics etc.

### Characteristics of stepper motor :-



\* The stepper motor has a permanent magnet rotor called shaft which is surrounded by the stator

\* The commonly used stepper motor will have four stator windings

\* These windings are called four phase (or) unipolar windings.

\* The stator is a magnet over which the electrical pulse of the coil is wound.

\* One end of the coil is connected either ground (or)  $\pm 5V$ .

\* The other end of the coil is provided with fixed sequence  $\therefore$  so, the stepper motor rotates in a particular direction.

\* The direction of rotation determined by the stator poles.

\* The stator poles is determined by the current pulses send through the coil.

step angle :-

$$\text{no. of steps per revolution} = \frac{360^\circ}{\text{step angle}}$$

$$\text{no. of steps per sec} = \frac{\text{rpm} \times \text{no. of steps per rev}}{60}$$

eg :-

step angle = 2

$$\text{no. of steps per revolution} = \frac{360^\circ}{2} = 180$$

Switching Sequence motor

two phase ON :-

STEP	A	B	C	D
1	1	0	0	1
2	1	1	0	0
3	0	1	1	0
4	0	0	1	1

clockwise

Anticlockwise

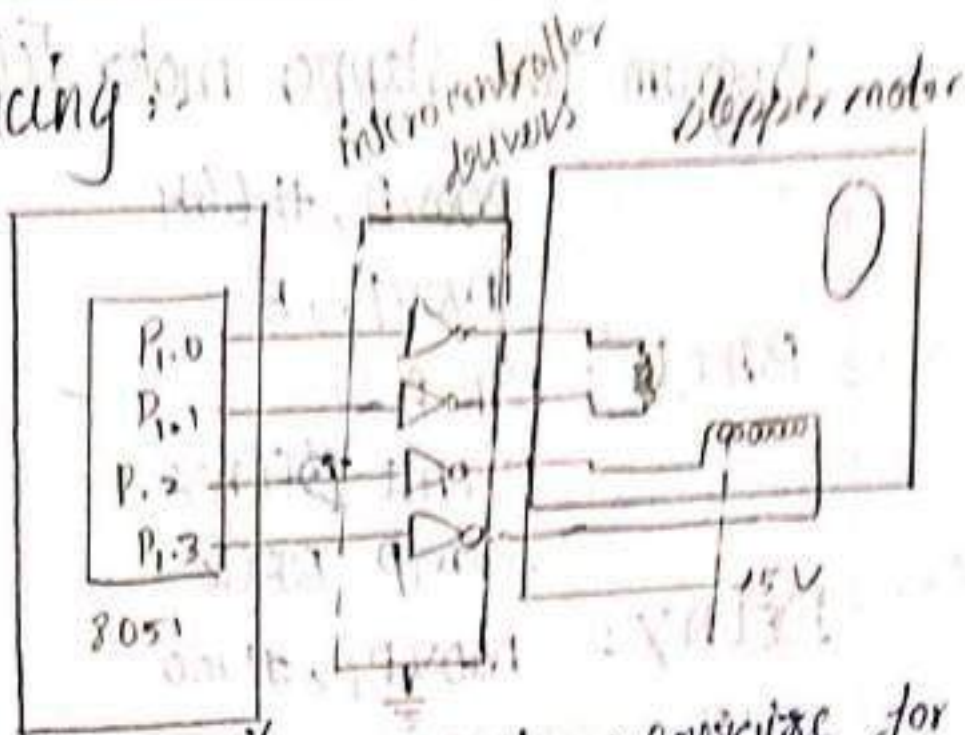
one phase ON :-

STEP	A	B	C	D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

clockwise

Anticlockwise

# Interfacing :



- \* The stepper motor can be energize for the rotates
- \* It can be done the single bit of switching sequence in one end of the coil.
- \* The 8051 has four ports P<sub>0</sub>, P<sub>1</sub>, P<sub>2</sub> & P<sub>3</sub>
- \* The port P<sub>1</sub> namely in 8051 microcontroller is P<sub>1.0</sub>, P<sub>1.1</sub>, P<sub>1.2</sub>, P<sub>1.3</sub> are connected to the stepper motor to the drivers.
- \* Data '1' is send through the port to energize.
- \* Data '0' is send through the port to de energize.
- \* The 8051 microcontroller can be program in stepper motor to rotates (clockwise direction (or) anticlockwise direction) both.

Program for stepper motor (clockwise)

MOVA, #66H

MOV P, A

BACK: RRA

CALL DELAY

SJMP BACK

DELAY: MOV R<sub>1</sub>, #100

UP<sub>1</sub>: MOV R<sub>2</sub>, #50

UP<sub>2</sub>: DJNZ R<sub>2</sub>, UP<sub>2</sub>

DJNZ R<sub>1</sub>, UP<sub>1</sub>

RET

Program for stepper motor [anticlockwise direction]

MOVA, #66H

MOV P, A

BACK: RLA

CALL DELAY

SJMP BACK

DELAY: MOV R<sub>1</sub>, #100

UP<sub>1</sub>: MOV R<sub>2</sub>, #50

UP<sub>2</sub>: DJNZ R<sub>2</sub>, UP<sub>2</sub>

DJNZ R<sub>1</sub>, UP<sub>1</sub>

RET

## Minimum mode Configuration :-

\* When a minimum mode pin-33  $V_{DD}/\bar{V}_{DD}$  is +5V.

\* In all control signals are given to the microprocessor chip itself.

\* There is a single microprocessor in minimum mode configuration.

\* Other components are latches, transceivers, memory, clock generator and I/O ports etc.

\* The latches are generally D-type flip flop like PC 8282

\* It is used for separation valid address from multiplexer Address data signal.

\* 3 latches are used for 20 address lines.

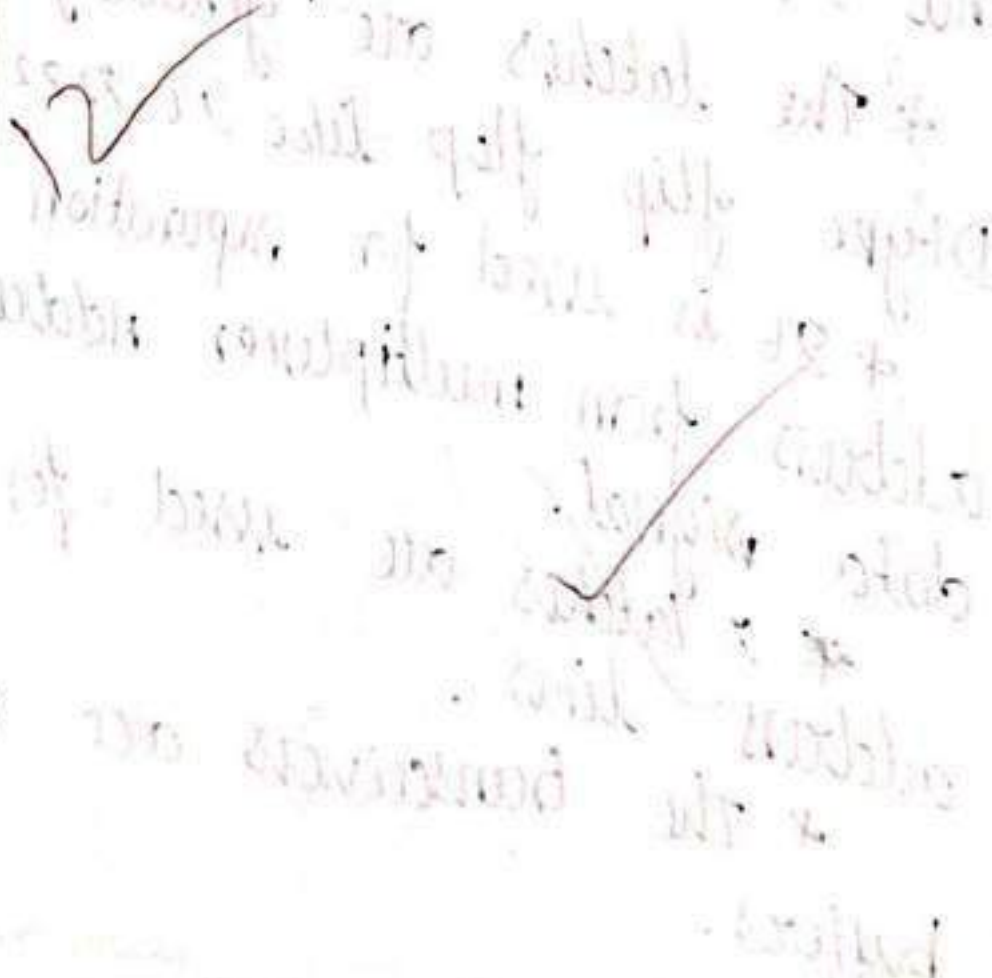
\* The transceivers are bidirectional buffers.

\* PE is used to separate data to multiplexer address signal.

\* The two buffers are two data lines.

\* The clock generator is used to generate the crystal oscillator and then it shaped and divide to more precisions.

\* So, it is used to the accurate timing sequence.



\* So, the  
categorized  
year



\* So, the timing diagram can be categorized into two parts Bus timing for read cycle, bus timing for write cycle.

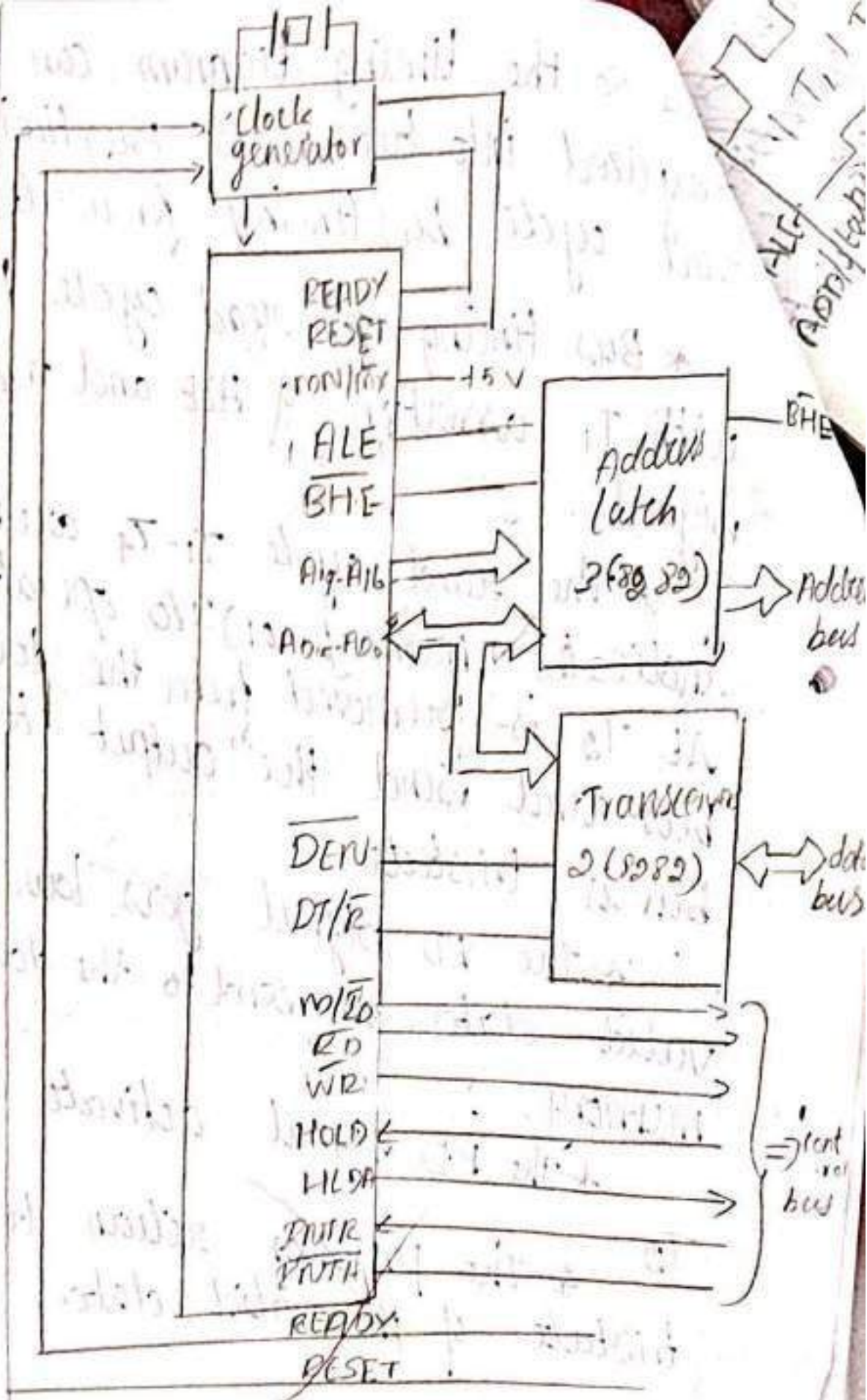
\* Bus timing for read cycle begins with  $T_1$  assertion of ALE and  $\overline{RD}$  signals.

\* The read cycle  $T_1 - T_4$  as  $\overline{RD}$  indicates memory or I/O operation. At  $T_2$  is removed from the local data bus and send the output to the bus is tristate.

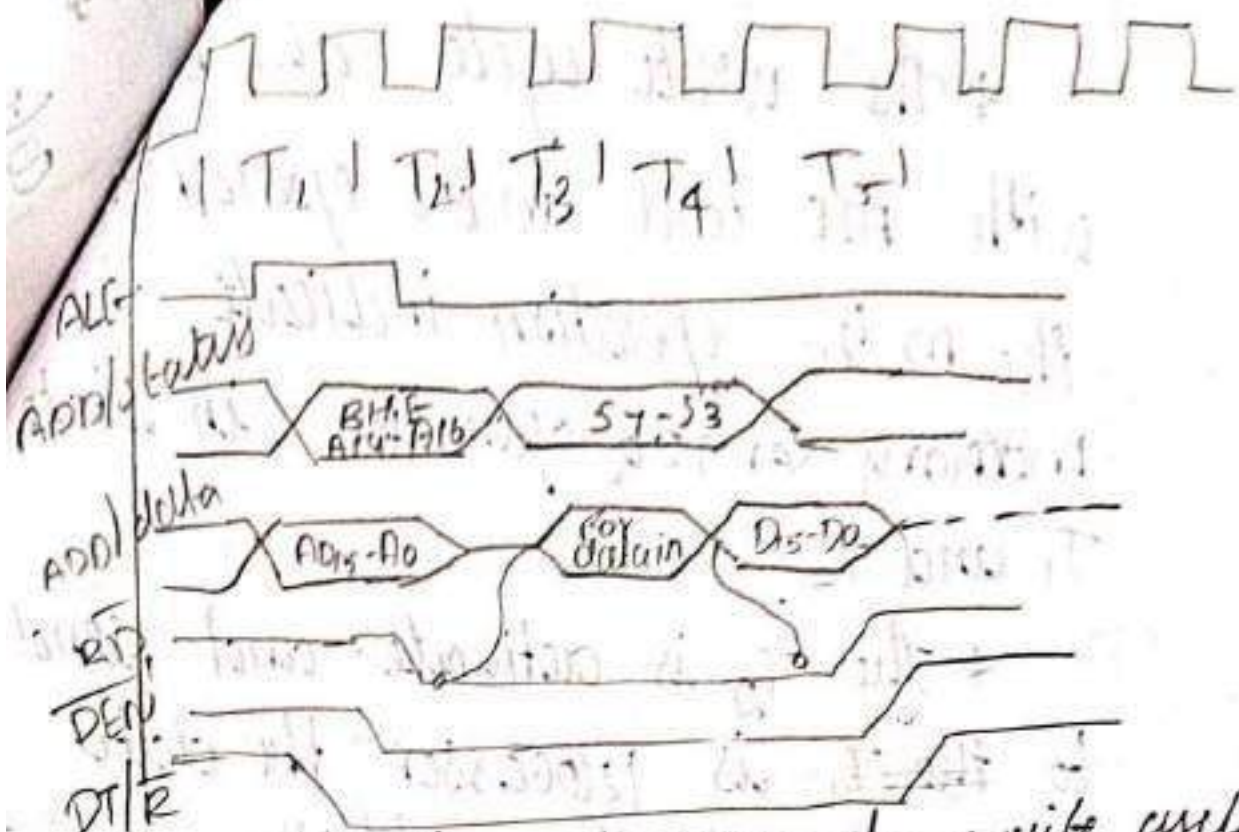
\* The  $\overline{RD}$  signal goes low, the valid data is send to the data memory.

\* The  $\overline{RD}$  signal activate in

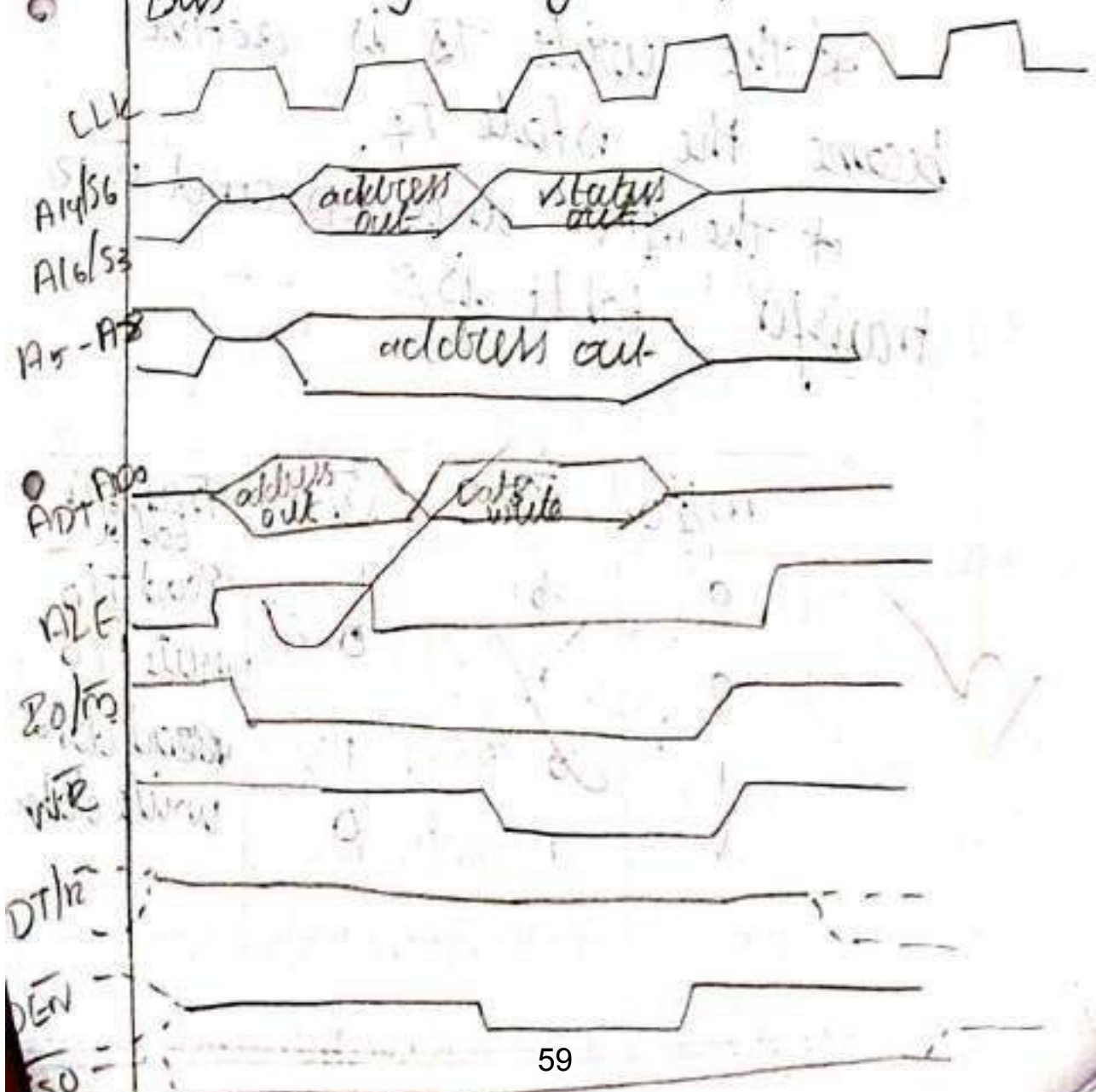
$T_3$ . \* The processor return to the tristate of the valid data.



Bus Timing for minimum mode :-  
 \* The opcode latches are 200 ns  
 cycle for similar.



Bus timing diagram for write cycle:



\* The write cycle also with ALE and  $\overline{M\overline{P\overline{O}}}$  operation. The  $\overline{M\overline{P\overline{O}}}$  operation indicate the memory or I/O operation in state  $T_1$  and  $T_4$ .

\* The  $T_2$  is activate and so to the  $T_1$  is processor the data is written to the address.

\* The write  $T_2$  is active because the state  $T_4$ .

\* The  $\overline{M\overline{P\overline{O}}}$  and  $\overline{RD}$  and  $\overline{WR}$  transfer table is,

$\overline{M\overline{P\overline{O}}}$	$\overline{RD}$	$\overline{WR}$	Transfer table
0	0	1	Read I/O
0	1	0	write I/O
1	0	1	Read data
1	1	0	write data

## 8254 :- Programmable Interval Timer

\* It is used for work in real life applications such that rate generator, timers and counting function.

\* eg:- BCD Binary generator, generation of square wave of desired frequency, rate generation etc.

Features of 8254 :-

\* 3 independent 16 bit down counters.

\* 8254 can handle the input from  $0\text{ Hz}$  to  $10\text{ MHz}$ .

\* counters can be programmed in different modes.

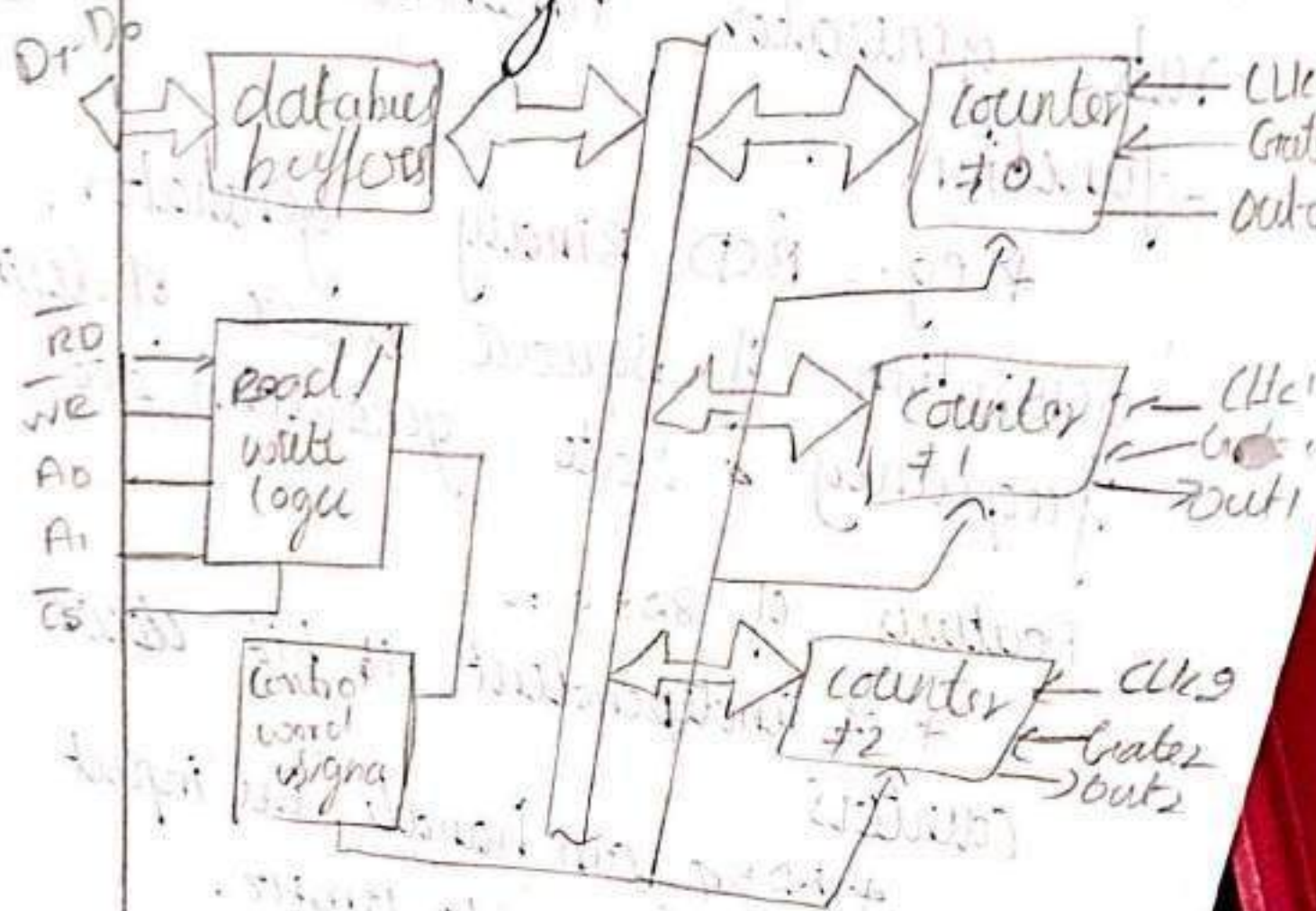
mode 0  $\rightarrow$  Interrupt on terminal count

mode 1  $\rightarrow$  programmable one-shot

mode 2  $\rightarrow$  rate generator

- mode 3 -> square wave generator
- mode 4 -> software triggered
- mode 5 -> hardware triggered

Block diagram:-



data bus buffer:-  
 \* It is a 8 bit, bidirectional data buffer used to interface the 8253 to system data bus.

scope

read/write logic:-  
 \* It is used to the control signal to the data bus in 8254 operation.

TS	A <sub>1</sub>	A <sub>0</sub>	$\overline{RD}$	$\overline{WR}$	
0	0	0	0	0	Read counter 0
	0	1	0	1	Read counter 1
	1	0	0	1	Read counter 2
	0	0	1	0	Write counter 0
	0	1	1	0	Write counter 1
	1	0	1	0	Write counter 2
	1	1	0	1	
	X	X	X	X	

Control word signal

SC <sub>1</sub>	SC <sub>0</sub>	RL <sub>1</sub>	RL <sub>0</sub>	$\overline{RD}$	$\overline{WR}$	BCD
-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----

SC → select counter

SC <sub>1</sub>	SC <sub>0</sub>	operation
0	0	select counter 0
0	1	select counter 1
1	0	select counter 2
1	1	illegal

BCD  $\rightarrow$  To select character

0  $\rightarrow$  Binary counter

1  $\rightarrow$  Binary coded decimal counter

RL  $\rightarrow$  Rotate Load

RL <sub>1</sub>	RL <sub>0</sub>	operation
0	0	Read/Write LS
0	1	Read/Write MSB
1	0	Read/Write MSB then MSB.
1	1	

$\bar{CS}$   $\rightarrow$  chip select

0  $\rightarrow$  chip is selected

1  $\rightarrow$  chip is not selected

modes

modes	operation
mode 0	Interrupt on terminal count
mode 1	programmable one shot
mode 2	state generator
mode 3	square wave generator
mode 4	software triggered strobe
mode 5	hardware triggered strobe



Final Course

# Architecture of 8051 microcontroller:-

## Features :-

- \* It is 8 bit CPU
- \* 4KB of ROM
- \* 128 bytes of RAM
- \* 21 special functions
- \* ~~two~~ 16 bits timers/counters
- \* 32 pins I/O port
- \* 64 KB of address space of the data memory
- \* 64 KB of address space of the program memory
- \* 8 bit addressable





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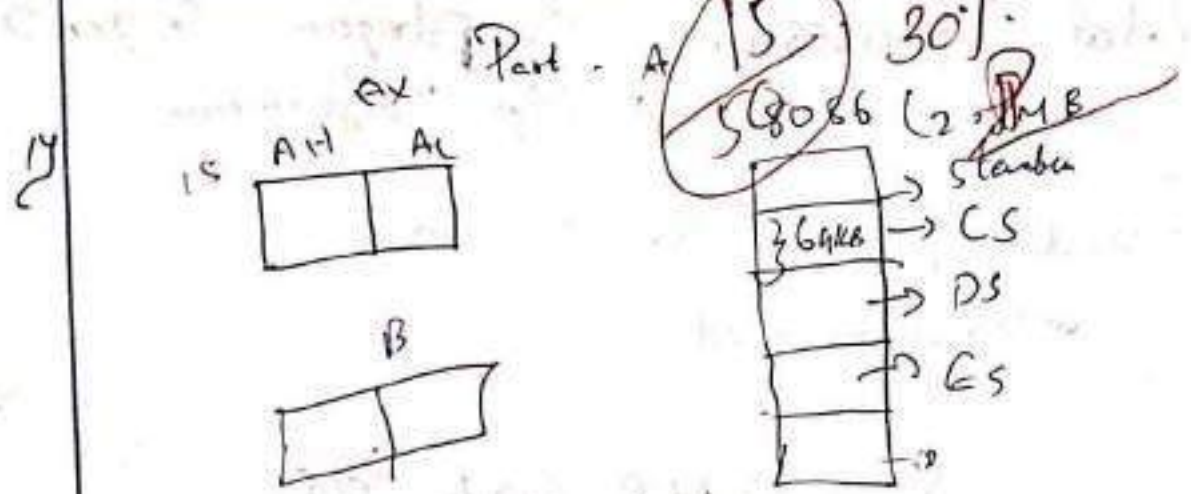
Permanent Affiliation for B.E. - Computer Science Engineering

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Name C. S. Theerth Kumar Roll No. 94020106306 Branch E.C.E

Year / Semester IV Subject Code / Title : EC 8691

Name of the Examination : Internal Exam I / II / III Total No. of Pages 06



Format of 8086 flag register

25 Linker

As we know that Linker has High essential Power for the transformation of the signal strength as we know is the job of the junction signal.

3) Solution

AR 4532

Adreno 660 - Snapdragon 865<sup>+</sup>

Latest processor \* Snapdragon 8gen2  
High Performance.

4 Operation of S<sub>0</sub>, S<sub>1</sub>, S<sub>2</sub> Pin in  
Maximum mod.

Sony IMR 624 lens.

S22 ultra Moon Camera

5 47 and 1 //

Explanation.. As we know As 8088

Hexa decimal can be changed  
by the A7 controller //

b)

### Architecture of 8086

The 8086 microprocessor consists of two equal units

- (i) BIU
- (ii) EU

BIU = Bus Interface unit

EU = Execution unit

#### BIU

It consists of

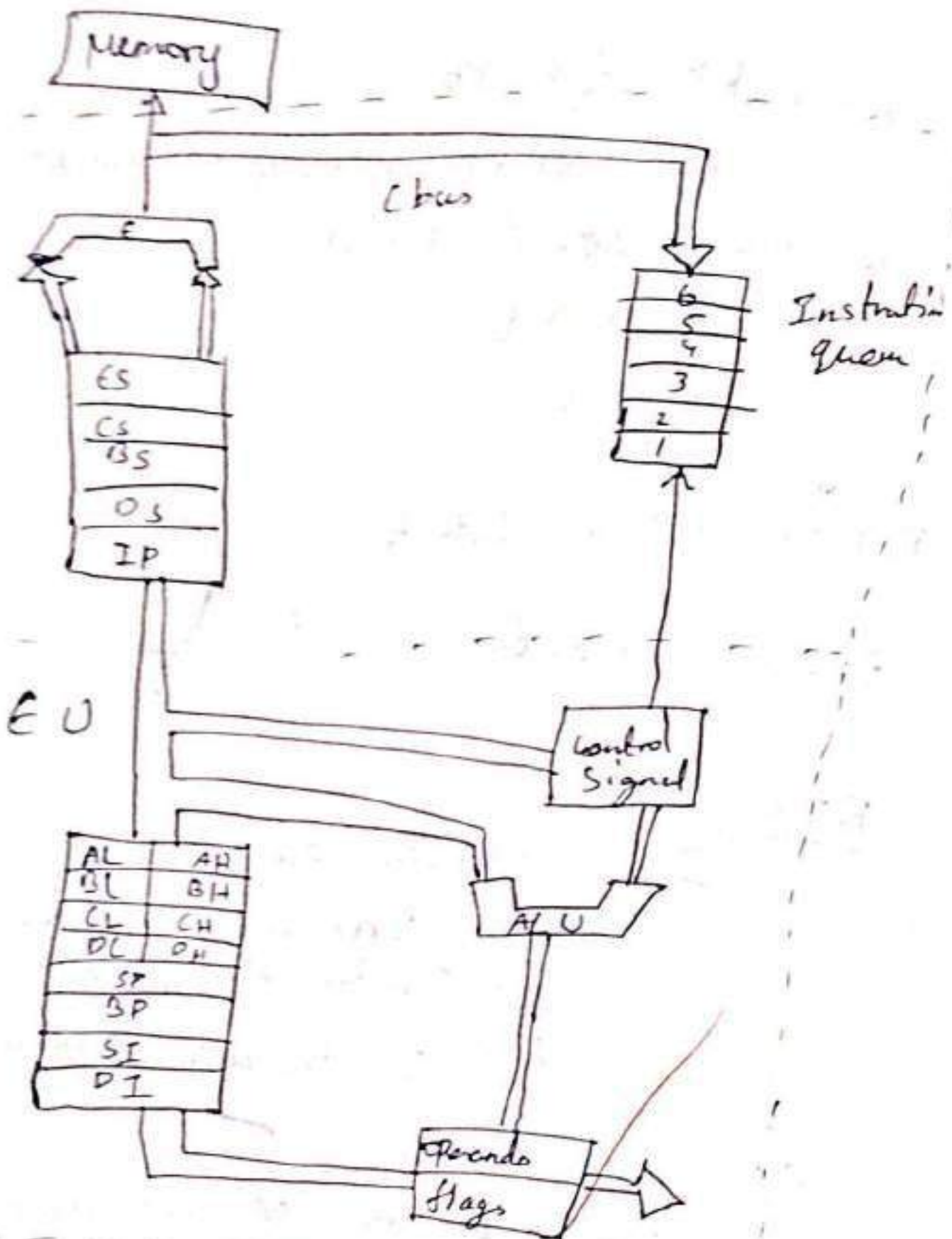
- (i) Segment register
- (ii) Instruction Pointer
- (iii) Instruction queue

#### EU

The execution of unit processes the data from the bus interface units. It consists of ALU

- (i) Register purpose register
- (ii) Index register
- (iii) Pointer
- (iv) Flag register

# BIU



Internal hardware architecture of 8086 microprocessor

## Construction of BIU,

The BIU is designed as the Bus Interface with Junction of the data transfer from the Memory as we know the Bus Bar has been

### Memory

The memory is the storage device of space to store the limited data signal on the storage for (or) Action the junction on the Bus Bar.

### C-Bus

The C-Bus is the signal strength transforming medium from several place to the

Functioning mechanism of the bus

as we know CS register

Instruction

BET register

The BET register is the  
Bit of storage device to

store the data through the  
Serial line of the Base  
Function System

(OS) ES - register

CS - register

BS - register

OS - register

IP - register

Now the signal  
has been transfer to the  
Position of the CPU.



## Instruction queue

The Instruction has been stored from the register bit as we can see on the above figure.

## EU - construction

- The EU is defined as the Execution Unit of the process of 8086 in the achievement of the hardware function of register and point flag register for storage
- Index

ALU = Arithmetic and Logic Units

## ALU

The ALU is the Programming language which can easily communicate through the computer.

## Control Signal

The control signal is act as the medium which can easily correct the input register and rectify and know the signal has been given to the Arithmetic and Logic unit.

## Flags

The flags are otherwise called as the operands for the Operational output units of the Operating system.

④ Minimum mode of 8086

a)

\* The minimum pin 33

is  $\overline{MN}/\overline{MX} = 1$  High

\* The another part are latches, memory, clock generator, logical signal, I/O devices, transceivers.

\* There is single microprocessor

\* It is a Arithmetic

latch enable

\* It receive the

latched data

Catches

The separates the address for the multiplexed data address

Transceivers

It is <sup>75</sup> separates the address

for the multiplexed data address.

## Memory

The user interface memory and

Storage memory

EEPROM → It is stage memory

RAM → It is user interface

memory

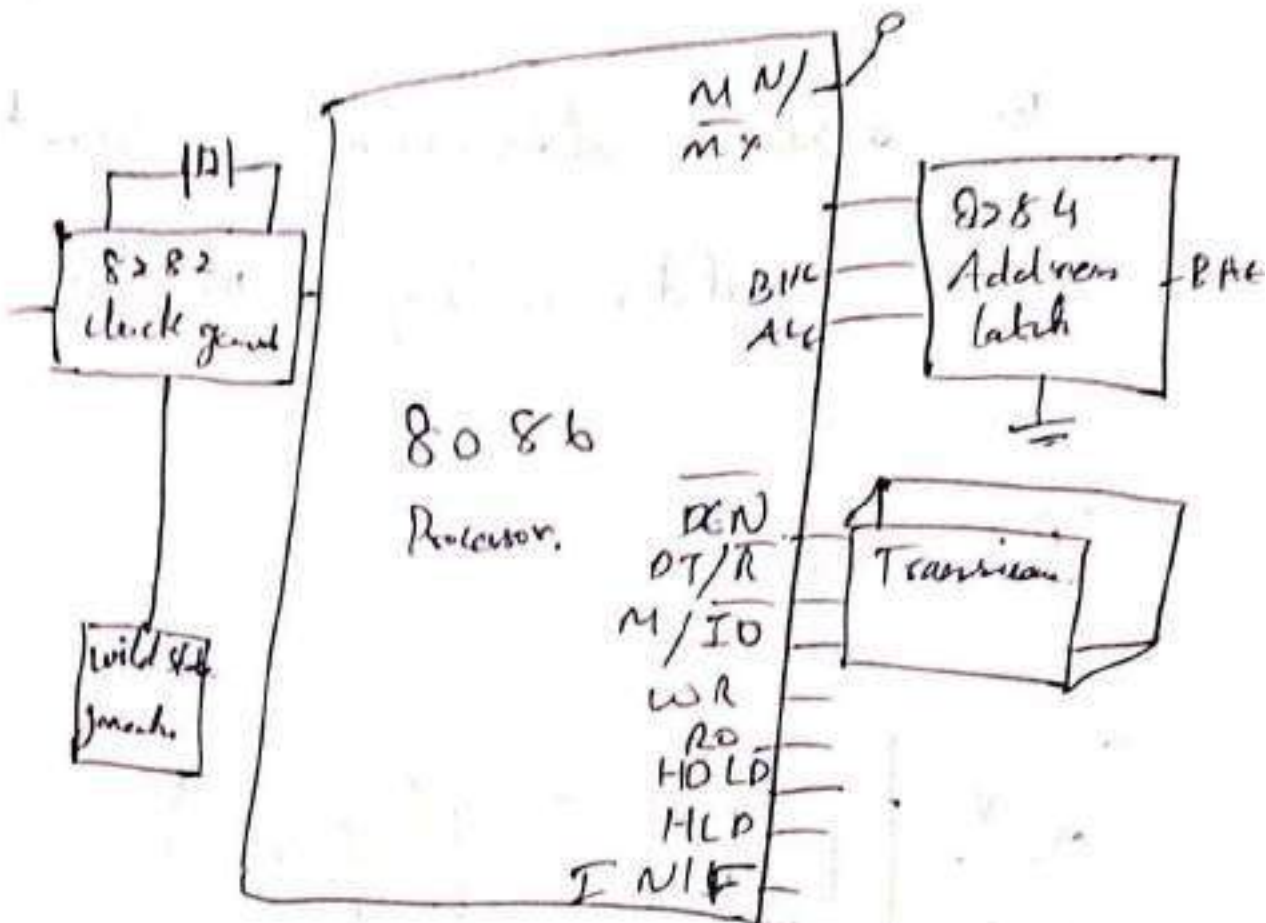
RAM = ~~A~~ Random access Memory

## Clock generator

It generates timing  
and clock phase

Minimum mode operation

of 8086



m

n

Construction

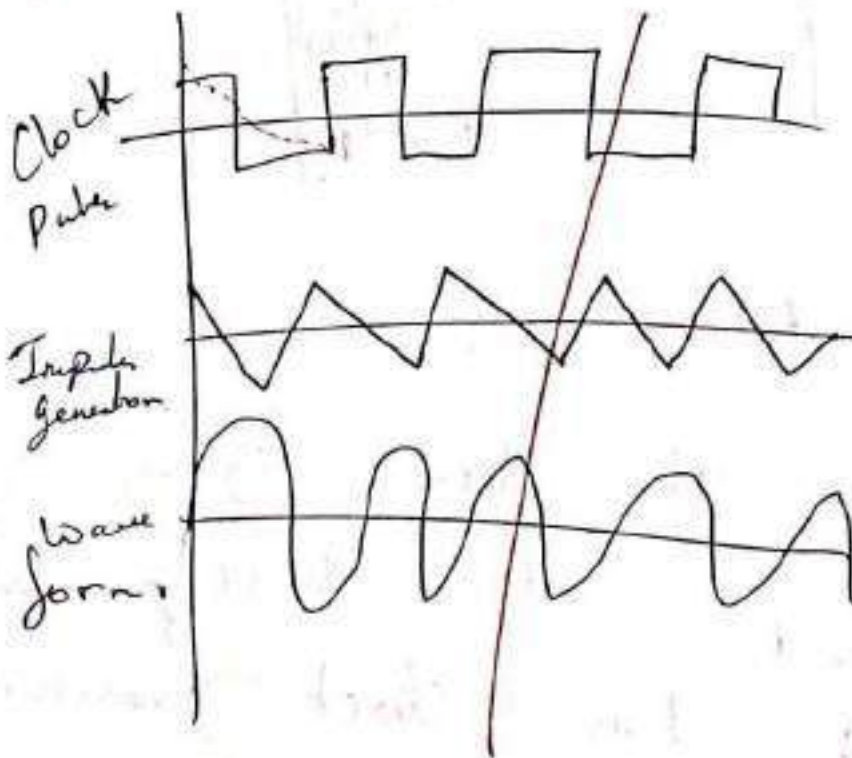
The above figure is about the 8086 processor. It has a clock generator. It will generate an impulse at several times difference.

Also it is connected to a  
State impulse generator to  
generate an pulse of 8284

is an addressing generator

of an addressing mode


Pulse generator



11/12/2020

7

**QUESTION BANK**  
**EC 8691 MICROPROCESSOR AND MICROCONTROLLER**  
**PART A-QUESTIONS WITH ANSWERS**  
**PART B-IMPORTANT QUESTIONS**

  
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# EC8691-MICROPROCESSOR AND MICROCONTROLLER

## UNIT-I

### THE 8086 MICROPROCESSOR

**SYLLABUS:** Introduction to 8086 – Microprocessor architecture – Addressing modes - Instruction set and assembler directives – Assembly language programming – Modular Programming - Linking and Relocation - Stacks - Procedures – Macros – Interrupts and interrupt service routines – Byte and String Manipulation.

**COURSE OBJECTIVE:** Know about the Architecture, addressing modes and instruction sets of 8086 Microprocessor.

### PART-A

#### 1. What is microprocessor?

A microprocessor is a multipurpose, programmable, clock-driven, register-based electronic device that reads binary information from a storage device called memory, accepts binary data as input and processes data according to those instructions, and provides result as output.

#### 2. What is Accumulator?

The Accumulator is an 8-bit register that is part of the arithmetic/logic unit (ALU). This register is used to store 8-bit data and to perform arithmetic and logical operations. The result of an operation is stored in the accumulator. The accumulator is also identified as register A.

#### 3. What is stack?

(EE2354 April/May 2013)

The stack is a group of memory locations in the R/W memory that is used for temporary storage of binary information during the execution of a program

#### 4. What is a subroutine program?

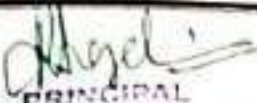
A subroutine is a group of instructions written separately from the main program to perform a function that occurs repeatedly in the main program. Thus subroutines avoid the repetition of same set of instructions in the main program.

#### 5. Define addressing mode.

Addressing mode is used to specify the way in which the address of the operand is specified within the instruction.

#### 6. Define instruction cycle.

It is defined as the time required to complete the execution of an instruction.

  
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- v. Machine control instruction
- vi. Flag manipulation instruction
- vii. Shift and rotate instruction
- viii. String instruction

**10. What is assembly level programming?**

A program called assembler is used to convert the mnemonics of instruction and data into their equivalent object code modules. The object code modules are further converted into executable code using linker and loader programs. This type of programming is called assembly level programming.

**11. What is a stack?**

Stack is a top-down data structure, whose elements are accessed using a pointer that is implemented using the SS and SP registers. It is a LIFO data segment.

**12. How is the stack top address calculated?**

The stack top address is calculated using the contents of the SS and SP register. The contents of stack segment (SS) register is shifted left by four bit positions (multiplied by 0h) and the resulted 20-bit content is added with the 16-bit offset value of the stack pointer (SP) register.

SS	-	5000H				
SP	-	2050H				
		SS	-	0101	0000	0000 0000
		10H * SS	-	0101	0000	0000 0000 0000
		SP	-	0010	0000	0101 0000
		Stack-top		0101	0010	0000 0101 0000
		Address		5	2	0 5 0

**13. What are macros?**

Macros are small routines that are used to replace strings in the program. They can have parameters passed to them, which enhances the functionality of the micro itself.

**14. How are constants declared?**

Constants are declared in the same way as variables, using the format:

```
Const-Label EQU 012h
```

When the constants label is encountered, the constant numeric value is exchanged for the string.

15. Write an assembly language program for a 16-bit increment and will not affect the contents of the accumulator.

```
MACRO inc16variable; Increment two bytes starting at "variable"
```

```
Local INC16 End
```

```
INC variable; Increment the low 8 bits PUSH ACC
```

```
MOV A variable; Are the incremented low 8 bits = 0?
```

```
JNZ INC 16 End
```

```
INC variable + 1
```

```
inc16 End; Yes—increment the upper 8 bits
```

```
POP ACC
```

```
END MAC
```

16. What will happen if a label within a macro is not declared local?

If a label within a macro is not declared local, then at assembly time, there will be two types of errors:

- I. The first will state that there are multiple labels in the source.
- II. The second will indicate that jump instructions don't know which one to use.

17. Write an assembly language program to load the accumulator with a constant value.

```
MACRO invert value
```

```
if (value==0)
```

```
MOV A, #1
```

```
else
```

```
clr A
```

```
end if
```

```
END MAC.
```

18. What is the difference between the microprocessor and microcontroller?

Microprocessor does not contain RAM, ROM and I/O ports on the chip. But a microcontroller contains RAM, ROM and I/O ports and a timer all on a single chip.

**19. What is assembler?**

The assembler translates the assembly language program text which is given as input to the assembler to their binary equivalents known as object code. The time required to translate the assembly code to object code is called access time. The assembler checks for syntax errors & displays them before giving the object code.

**20. What is loader?**

The loader copies the program into the computer's main memory at load time and begins the program execution at execution time.

**21. What is linker?**

A linker is a program used to join together several object files into one large object file. For large programs it is more efficient to divide the large program modules into smaller modules. Each module is individually written, tested & debugged. When all the modules work they are linked together to form a large functioning program.

**22 .Explain ALIGN & ASSUME.**

(Nov/Dec 2010, April/may2011)

The ALIGN directive forces the assembler to align the next segment at an address divisible by specified divisor. The format is ALIGN number where number can be 2,4, 8 or 16. Example ALIGN 8. The ASSUME directive assigns a logical segment to a physical segment at any given time. It tells the assembler what address will be in the segment registers at execution time. Example ASSUME CS: code, DS: data, SS: stack

**23. Explain PTR & GROUP**

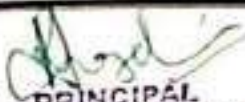
A program may contain several segments of the same type. The GROUP directive collects them under a single name so they can reside in a single segment, usually a data segment. The format is Name GROUP Seg-name,....Seg-name PTR is used to assign a specific type to a variable or a label. It is also used to override the declared type of a variable.

**24. Explain PROC & ENDP (April/May 2010)**

PROC directive defines the procedures in the program. The procedure name must be unique. After PROC the term NEAR or FAR are used to specify the type of procedure. Example FACT PROC FAR.ENDP is used along with PROC and defines the end of the procedure.

**25. Explain SEGMENT & ENDS**

An assembly program in .EXE format consists of one or more segments. The starts of these segments are defined by SEGMENT and the end of the segment is indicated by ENDS directive. Format Name SEGMENT.

  
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**26. Define SOP**

(Nov/Dec2010)

The segment override prefix allows the programmer to deviate from the default

Segment Eg : MOV CS: [BX], AL

**27. Define variable.**

A variable is an identifier that is associated with the first byte of data item. In assembly language statement: COUNT DB 2011, COUNT is the variable.

**28. What are procedures?**

Procedures are a group of instructions stored as a separate program in memory and it is called from the main program whenever required. The type of procedure depends on where the procedures are stored in memory. If it is in the same code segment as that of the main program then it is a near procedure otherwise it is a far procedure.

**29. Explain the linking process.**

A linker is a program used to join together several object files into one large object file. The linker produces a link file which contains the binary codes for all the combined modules. It also produces a link map which contains the address information about the link files. The linker does not assign Absolute addresses but only relative address starting from zero, so the programs are relocatable & can be put anywhere in memory to be run.

**30. Compare Procedure & Macro.(April/May2011)**

Procedure	Macro
Accessed by CALL & RET instruction during program execution	Accessed during assembly with name to macro when defined
Machine code for instruction is put only Once in the memory	Machine code is generated for instruction each time when macro is called
With procedures less memory is required	With macro more memory is required
Parameters can be passed in registers, memory locations or stack	Parameters passed as part of statement Which calls macro

31. What is the maximum memory size that can be addressed by 8086? (April/May 2014)  
(Nov/Dec 2014)

In 8086, a memory location is addressed by 20 bit address and the address bus is 20 bit address and the address bus is 20 bits. So it can address up to one megabyte ( $2^{20}$ ) of memory space.

32. How many data lines and address lines are available in 8086?

Address lines= 20 bit address bus

Data lines= 16 bit data bus

33. What information is conveyed when Qs1 and Qs0 are 01?

Qs1 and Qs0 are output signals that reflect the status of the instruction queue. When Qs1 and Qs0 are 01, then queue has first byte of an opcode.

34. What is the addressing mode of MOV AX, 55H (BX) (SI) ?

MOV AX, 55H (BX) (SI) – Base Indexed memory addressing mode.

35. What are the 8086 interrupt types?(Apr/May 2015)

Dedicated interrupts

- Type 0: Divide by zero interrupt
- Type 1: Single step interrupt
- Type 2: Nonmaskable interrupt
- Type 3: Breakpoint
- Type 4: Overflow interrupt

Software interrupts: Type 0-255


36. What is interrupt service routine?[NOV/DEC 2011]

Interrupt means to break the sequence of operation. While the CPU is executing a program an interrupt breaks the normal sequence of execution of instructions & diverts its execution to some other program. This program to which the control is transferred is called the interrupt service routine.

37. Calculate the physical address for fetching the next instruction to be executed, in 8086?

The physical address is obtained by appending four zeros to the content present in CS register and then adding the content of IP register with the above value.

For example, assuming the content of

  
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19) CS = 1200 H

IP = 0345 H

CS = 0001 0010 0000 0000 0000

0000 0011 0100 0101

-----  
0001 0010 0011 0100 0101 – Physical address = 12345 H

38. If the execution unit generates effective address of 43A2 H and the DS register contains 4000 H. What will be the physical address generated by the BIU? What is the Maximum Size of the data segment?

Effective Address      43A2H

Physical Address      40000H

Maximum size of the DS is  $2^{16}$

39. Calculate the physical address, when segment address is 1085H and effective address is 4537H. [Nov/Dec 2015]

Segment address - 1085H


Effective address - 4537H

-----  
Physical address - 14D87H  
-----

40. Show how the 2 byte INT instruction can be applied for debugging. [Nov/Dec 2015]

INT type

The INT instruction is used as a debugging and in case where single stepping provides more detail then is wanted, by inserting INT instructions at key points called break points.

  
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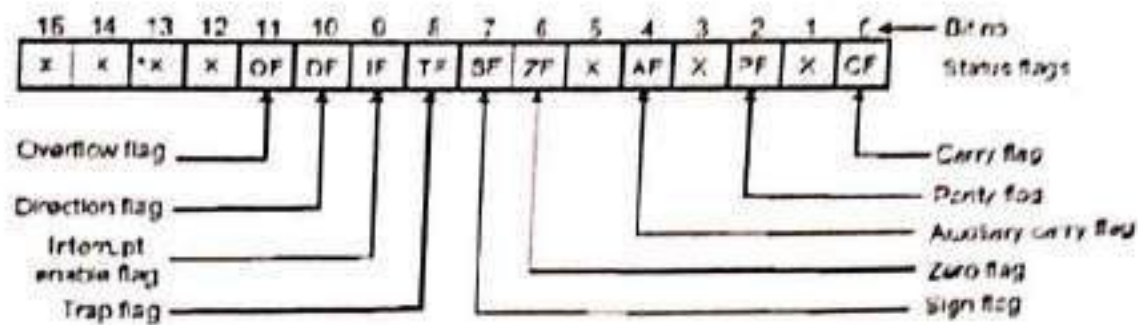


Fig. 11.0: Status flags of intel 8086

- OF - Overflow Flag. Set if signed number exceeds capacity of result. ...
- DF - Direction Flag. Set by user to indicate a direction (0=forward, 1=backward) ...
- IF - Interrupt Flag. Set by user to disable hardware interrupts temporarily. ...
- TF - Trap Flag. Used by debuggers.
- SF - Sign Flag. ...
- ZF - Zero Flag. ...
- AF - Aux. ...
- PF - Parity Flag.

PART-B 4 C

1. (a) Write an assembly language program in 8086 to search the largest data in the array(6) C (April/May 2011)  
(b) Explain the various status flags in 8086. U (Nov/Dec2011)(6)
2. (a) Discuss the various addressing modes of 8086. U (April/May2011) (Nov/Dec 2014) (8)  
(b) Explain the following assembler directive in 8086 (6). U (April/May2013)(Apr/May 2015)  
i. ASSUME ii. EQU iii. DW iv. DD
3. (a) Write short notes on Macro(6) C(April/May 2012)  
(b) Explain the function of assembler directives. U(10) (April/May2011) (Nov/Dec 2014)
4. Explain the architecture of 8086. U(16) (Nov/Dec2014), (April/May2011) [Nov/Dec2015] (8)

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5. (a) Explain the register organization of 8086. U(10)(April/May2013)  
(b) Explain the pin diagram of 8086 (6) U
6. Discuss the instruction set of 8086 in detail (8) (April/May 2011) U
7. Explain the interrupt and types?(8) (Nov/Dec2010) (April/May 2011) U
8. Explain briefly about the internal hardware architecture of 8086 microprocessor with a neat diagram (Apr/May 2015) (10) U
9. Write an assembly language program in 8086 to convert BCD data – binary data. C (Apr/May 2015) (6)
10. Explain briefly about Interrupt handling process in 8086. (Apr/May 2015) (8) U
11. Explain in detail about the interrupts and interrupt service routines of 8086. [Apr/May 2015] [Nov/Dec 2015] U
12. (I) Explain the Data transfer, arithmetic and branch instructions with examples.(9) U  
(II) Write an 8086 ALP to find the sum of numbers in an array of 10 elements. (7) [May/June 2016]
13. Define interrupts and their types. Write in detail about interrupt service routine. (16) C [May/June 2016]
- COURSE OUTCOME:** Learnt the architecture, Instruction set and Programming of 8086 Microprocessor.



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**UNIT-II MICROPROCESSORS AND  
MICROCONTROLLERS  
PART A**

1. *What are the two modes in which 8086 operates?*

8086 operates in two modes

3. Minimum mode and
4. Maximum mode.

2. *Explain the difference between minimum mode and maximum mode of operation.*

Minimum mode	Maximum mode
1. When 8086 is operating in minimum mode the pin MN/MX will be connected to VCC	When 8086 is operating under maximum mode the pin MN/MX will be connected to GND.
2. It is used in single processor environment	It is used in multi processor environment

3. *State the functions of queue status lines QS0 and QS1 in 8086 microprocessor.*

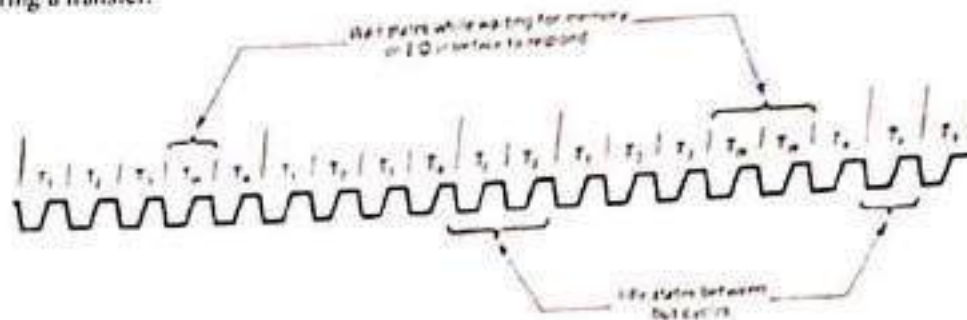
QS1	QS0	Function
0	0	Queue is in idle state
0	1	First byte of opcode has entered into the queue
1	0	Queue empty
1	1	Subsequent byte of opcode has entered into the queue



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**4. Define idle cycle and wait state.**

If the bus is to be inactive after the completion of a bus cycle, then the gap between successive cycles is filled with idle state clock cycles represented by  $T_1$ . Wait states are inserted between  $T_1$  and  $T_2$  when a memory or I/O interface is not able to respond quickly enough during a transfer.



**5. What are the three principal types of I/O programming?**

The three principal types of I/O are:

1. Programmed I/O
2. Interrupt I/O
3. Block transfers.

**6. What are the ways in which the data can be transferred to or from the port?**

The transfer of data to or from a port can be done in two ways.

1. To execute an instruction that causes a single byte or word to be transferred
2. To execute a sequence of instructions that causes a special system component associated with the interface to transfer a sequence of bytes or words to or from a pre designated block of memory locations.

**7. What is meant by bus cycle?**

The activity involved in transferring a byte or word over the system bus is called a bus cycle.

**8. Define cycle stealing.**

During any given bus cycle, one of the system components connected to the system bus is given control of the bus. This component is said to be the master during that cycle and the component it is communicating with is said to be the slave. The CPU with its bus control logic is normally the master, but other specially designed components can gain control of the bus by sending a bus request to the CPU. After the current bus cycle is completed the CPU will

  
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return a bus grant signal and the component sending the request will become the master. Taking control of the bus for a bus cycle is called cycle stealing.

9. Give the difference between uniprogramming and multiprogramming.

Uniprogramming	Multiprogramming
1. When processes are executed in a serial fashion, the system is called a uniprogramming system.	When processes are executed in a time multiplexed fashion, the system is called a multiprogramming system
2. In such systems, normally only one process is stored in the memory at a time and the next process is not loaded for execution until the current one is terminated.	For a multiprogramming environment, the code for two or more processes is in memory at the same time and is executed.

10. What are the three states in process management.

1. **Running**-When the process is currently being executed by the CPU.
2. **Blocked**-When the execution of the process cannot be continued because it is waiting for an event to occur, e.g., it is waiting for the completion of an I/O operation.
3. **Ready**-When the execution of the process can be resumed any time. For example, the I/O process has been waiting has finished and the processing is able to continue.

11. Define semaphore.

A flag used to reserve a shared resource is called a semaphore and the operations of requesting and releasing the resource are commonly known as the P and V semaphore operators. If FLAG = 1 indicates that the resource is free and FLAG = 0 indicates it is busy.

12. Define bus and explain what is meant by internal bus and external bus.

A set of conductors used for communicating information between the components in a computer system is called a bus. If a bus connects two minor components within a major component (e.g., the control unit to the set of working registers within the CPU), it is called an internal bus. When a bus connects two major components, such as a CPU and an interface, it is called an external bus.

13. What is meant by multiprocessing system?

If a system includes two or more components that can execute instructions simultaneously, it is called a multiprocessing system. The added processors could be special purpose processors which are specifically designed to perform certain tasks efficiently, or other general purpose processors. For example, due to the 8086's limited data width and its lack of floating point arithmetic instructions, it requires many instructions to perform a single floating point operation.



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- If any failure occur, it is easier and cheaper to find and replace the malfunctioning processor than it is to find and replace the failing part in a complex processor.

**14. What are the three basic configuration of multiprocessor configuration.**

Multiprocessing features are provided in maximum mode to accommodate three basic configurations. They are the

1. Coprocessor configuration
2. Closely coupled configurations
3. Loosely coupled configurations.

**15. What are the advantages of loosely coupled configuration?**

A loosely coupled configuration provides the following advantages:

1. High system throughput can be achieved by having more than one CPU.
2. Each bus master module is an independent unit and normally resides on a separate PC board. Therefore, a bus master module can be added or removed without affecting the other modules in the system.
3. A failure in one module normally does not cause a breakdown of the entire system and the faulty module can be easily detected and, replaced.
4. Each bus master may have a local bus to access dedicated memory or I/O devices so that a greater degree of parallel processing can be achieved.

**16. What are the three schemes that are used for establishing priority in loosely coupled configuration? (or) State the ways by which bus contention problem can be removed.**

There are three schemes for establishing priority:

1. Daisy chaining
2. Polling
3. Independent requesting.

**PART B**

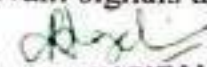
1. With necessary diagram explain in detail about multiprocessor configuration?
2. Describe the maximum mode signals, and maximum mode system configuration of 8086 microprocessor in detail.(16)
3. Describe the minimum mode signals, and minimum mode system configuration of 8086 microprocessor in detail.(16)
4. Explain maximum mode bus cycle in 8086 microprocessor. (8)



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## PART B + C


1. Discuss the maximum mode configuration of 8086 by with a neat diagram. Mention the functions of the various signals. (Apr/May 2015, Apr/May 2018) (Understand)
2. Explain in detail about the system bus timing of 8086. (May/June 2016, NOV/DEC 2016, APRIL/MAY 2017) (Understand)
3. Explain the multiprocessor configuration of 8086. (Nov 07, May 07, NOV/DEC 2016, Apr/May 2018) (Understand)
4. Explain the architecture of 8087 with neat block diagram. (May 07, May 08, May 10, May 12, Nov 11) (Understand)
5. Explain the 8087 co-processor data format. (May 10, May 21, Nov 10) (Understand)
6. Explain the architecture of 8089 with neat block diagram. (May 07, May 10, May 12, May 14) (Understand)
7. Explain in detail about closely coupled and loosely coupled configuration. What are the relative advantages and disadvantages? (Nov 07, Nov 10, May 08, Nov 11) (Understand)
8. Compare closely coupled configuration with loosely coupled configuration. (Apr/May 2015) / Distinguish between closely coupled and loosely coupled multiprocessor configuration (Nov /Dec 2018) [Nov/Dec 2021) (Analyze)
9. Discuss the schemes used to solve bus arbitration problem in multiprocessors.
10. Explain the exception handling feature of 8087. (Nov/Dec 10) (Understand)
11. Explain the closely coupled configuration of multiprocessor configuration with suitable example. (May 2014, APRIL/MAY 2017) (Understand)
12. Write a 8086 assembly language program to check whether the given string is palindrome or not. (Apr/May 2015) (Create)
13. Explain the execution steps of 8087. (May 2014) (Understand)
14. With neat diagram explain the minimum mode of operation of 8086 (Nov/Dec 2015) (Understand)
15. Define loosely coupled system. Explain the schemes used for establishing priority (Nov/Dec 2015) (Remember)
16. Explain the following: i. multiprocessor system ii. Coprocessor iii. Multiprogramming iv. Semaphore (May/June 2016) (Understand)
17. Draw the diagram showing address demultiplexing for 8086. Explain the use of each IC in the system and relevant pins and signals. NOV/DEC 2019) (Remember)
18. Draw the timing diagram for the "Memory Read" machine cycle of 8086. Explain the function of the relevant signals and discuss how

  
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- each signal changes in the progress of the machine cycle.(NOV/DEC 2019) (Understand)
19. Explain the system bus structure of 8086. Draw the timing diagram for interrupt acknowledgement cycle. (Nov/Dec 2017)(Understand)
20. Explain the loosely looped configuration with neat diagram. (Nov/Dec 2017) (Understand)
21. What do you understand from system bus structure ? explain (Nov/Dec 2018)(Understand)
22. With neat block diagram , explain the architecture of 8086 in maximum mode configuration. Also explain the Bus Timing diagram for input and output transfer on a maximum mode. (Apr / May 2019) (Understand)
23. Explain the interrupt system based on multiple 8259-with necessary block diagram. (Apr / May 2019)(Understand)
24. Examine all the pins functions of 8086 processor with neat pin diagram (Understand) (Nov/Dec 2021)

Part – C

1. Based on what you know, how would you explain I/O processor(Understand)
2. Explain short notes about the advanced processors (Understand)

  
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## UNIT - III I/O INTERFACING

### Part - A

1. What are the modes of operation of 8255?  
(Understand)

- > BSR Mode
- > IO Mode
- Mode 0
- Mode 1
- Mode 2

2. List the steps in the general algorithm for ADC interfacing?(Understand)

- o Ensure the stability of analog input applied to the ADC.
- o Issue start of conversion (SOC) pulse to ADC.
- o Read end of conversion (EOC) signal to mark the end of conversion process.
- o Read analog data output of the ADC as equivalent digital output.

3. Give the various modes & applications of 8254 timer (or) List the six modes of operation of 8253?(Apr/May 2015, Apr/May 2018)  
[NOV/DEC 2021](Understand)

- ❖ Mode 0 (Interrupt on terminal count) Mode 1 (Programmable mono-shot)
- ❖ Mode 2 (Rate generator)
- ❖ Mode 3 (Square wave generator)
- ❖ Mode 4 (Software triggered strobe)
- ❖ Mode 5 (Hardware triggered strobe)

4. List the command words of 8259A  
(Understand)

Initialization command word & Operation command word

5. What are the operational modes of 8279?

- Input (Keyboard) mode &
- Output (Display) mode

(Remember)

6. What are three modes of data transmission?

- Simplex
- Half duplex &
- Full duplex

(Remember)

7. List the transfer modes of 8237?



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(Understand)

- Single transfer mode
- Block transfer mode
- Demand transfer mode
- Cascade mode
- Memory to memory transfer

8. List the commands that can be executed by 8237? (Understand)

- Clear First / Last Flip flop
- Clear Mask Register
- Master Clear Command

9. List the salient features of Mode0 of 8255?

(Remember)

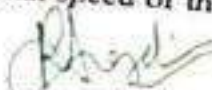
- ✓ Two 8 bit ports (Port A and Port B) and two 4 bit ports (Port C upper and lower) are available. The two 4 bit ports can be collectively used as third 8 bit port.
- ✓ Any port can be used as an input or output port.
- ✓ Output ports are latched. Input ports are not latched.
- ✓ A maximum of 4 ports are available so that overall 16 I / O configurations are possible.

10. State the features of 8255 in Mode1?

(Apply)

- Group A and Group B are available for strobed data transfer.
- Each group contains one 8bit data I / O port and one 4 bit control / data port.
- 8bit data port can be either used as input or output port.
- Out of 8bit portC, PC0 – PC2 are used to generate control signals for port B, PC3 – PC5 are used to generate control signals for port A. PC6, PC7 may be used as independent data lines. State the salient features of Mode2 of 8255? (Apply)
- Single 8 bit port in group A is available
- 8bit port is bidirectional and a 5bit control port is available.
- 3 I / O ports are available at port C, PC2 – PC0
- Inputs and outputs are both latched.
- 5 control bits of portC (PC3 – PC7) is used for generating / accepting handshake signals for the 8bit data transfer on portA.

11. What is the disadvantage in keyboard interfacing using ports? (Understand) The disadvantage in keyboard interfacing using ports is that most of the processor time is utilized in keyboard scanning and debouncing. As a result the computational speed of the processor will be reduced.



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19. What are the control words of 8251 and what are its functions?(Analyze) The control words of 8251 are mode word and command word. The mode word informs 8251 about the baud rate, character length, parity and stop bits. The command word can be send to enable the data transmission and reception.

20. What are the information that can be obtained from the status word of 8251?(Remember)

The CPU to check the readiness of the transmitter or receiver and to check the character synchronization in synchronous reception can read the status word. It also provides information regarding various errors in the data received. The various error conditions that can be checked from the status word are the parity error, overrun error and framing error.

21. What is baud rate?

(Remember)

The baud rate is defined at which the serial data are transmitted. Baud rate is defined as  $1/(\text{the time for a bit cell})$ . In some systems one bit cell has one data bit, then the baud rate and bits/sec are same.

22. What are the different types of data transfer scheme?

(Understand)

The different types of data transfer scheme are

- Synchronous u data transfer scheme.
- Asynchronous data transfer scheme
- Interrupt driven data transfer scheme.

23. What are the different types of DMA data transfer scheme? (Understand)

The different types of DMA data transfer scheme are

- Cycle stealing DMA
- Block or burst mode DMA
- Demand transfer mode DMA

24. What is the need for interrupt controller?

(Remember)

The interrupt controller is employed to expand the interrupt inputs. It can handle the interrupt request from various devices and allow one by one to the processor.

25. List some of the features of INTEL 8259.

(Understand)

- It manage eight interrupt request
- The interrupt vector addresses are programmable
- The priorities of interrupts are programmable.
- The interrupt can be masked or unmasked individually.

  
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12. What is the advantage in using INTEL 8279 for keyboard and display interfacing?

(Understand)

When 8279 is used for keyboard and display interfacing, it takes care of the entire task involved in keyboard scanning and display refreshing. Hence the processor is relieved from the task of keyboard scanning, debouncing, keyboard generation and display refreshing and the processor time can be more effectively used for computing.

13. What is a programmable peripheral device?

(Remember)

If the functions performed by a peripheral device can be altered or changed by a program instruction, then the peripheral device is called programmable device. Usually the programmable devices will have control registers. The device can be programmed by sending control word in the prescribed format to the control register.

14. What is synchronous data transfer scheme?

(Remember)

In synchronous data transfer scheme, the processor does not check the readiness of the device after a command have been issued for read/write operation in this scheme the processor will request the device to get ready and then read/write to the device immediately after the request.

15. What is asynchronous data transfer scheme?

(Remember)

In asynchronous data transfer scheme, first the processor sends a request to the device for read/write operation. Then the processor keeps on polling the status of the device. Once the device is ready, the processor executes a data transfer instruction to complete the process.

16. What are the operating modes of 8255?

(Understand)

The port of 8255 can be programmed to work in any one of the following operating modes as input or output port.

Mode-0 : simple I/O port, Mode-1 : handshake I/O port, Mode-2:bi-directional I/O port

17. What are the functions performed by port-C of 8255?

(Analyze)

- The port-C pins are used for handshake signals.
- Port-C can be used as an 8-bit parallel I/O port in mode-0
- It can be used as two numbers of 4-bit parallel port in mode-0
- The individual pins of port-C can be set or reset for various control applications.

What is USART? (Remember)

The device which can be programmed to perform synchronous or asynchronous serial communication is called USART (Universal Synchronous Asynchronous Receiver Transmitter). The INTEL 8251 is an example of USART.

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18. What are the functions performed by INTEL 8251?

(Analyze)

The INTEL 8251 is used for converting parallel data to serial or vice-versa. The data transmission or reception can be either asynchronous or synchronous. The 8251 can be used to interface MODEM and or synchronously. The 8251 can be used to interface MODEM and establish serial communication through MODEM over telephone lines.

## PART B

1. Explain how D/A and A/D interfacing done with 8086 with an application. (Apr/May 2015) (Apply)
2. What is DMA? Explain the DMA based data transfer using DMA controller. (Apr/May 2015) (Remember)
3. Draw the block diagram of traffic light control system using 8086. (Apr/May 2015) (Apply)
4. Write the algorithm & assembly language program for traffic light control system. (Apr/May 2015) (Create)
5. Explain the block diagram of 8255 (PPI) in detail. (Nov 08, Nov 05, Nov 6, May 12, May 08)[Nov/Dec 2021] (Understand)
6. Explain the operating modes and control word format of 8255. (Nov 12) (Apply)
7. Explain the block diagram of 8251(serial Communication) in detail (May 10, May 06, May 07) (Apply)
8. Explain the control word format of 8251. (May 10, May 06, May 12, Nov 11)(A)
9. Explain the block diagram of 8253(timer) with control word and also explain the operating modes with timing diagram. (May 10, Nov 08, May 12, Nov 10, Nov 11, May 7) (May/June 2016) (Apply)
10. Explain the block diagram of 8279(Keyboard/display) in detail.(Nov 07, May 05, Nov 08, Nov 0, Nov 11, May 13)[Nov/Dec 2021] (Apply)
11. Explain the block diagram of 8259(PIC) in detail.(May 10, May 06, May 12, Nov 10, May 08, May 07, Nov 11) (Apply)
12. Explain the block diagram of 8237(DMA) in detail.(Nov 07, May 06, Nov 10, May 12, May 08, May 07, May 12) (Apply)
13. Draw the schematic for interfacing a stepper motor with 8085 microprocessor. (May 12)(Create)
14. Explain in detail about the temperature control by interfacing with 8085.(Nov 07, May 08) (Apply)
15. Explain the (i) modes of operation of timer (ii) operation of interrupt controller.(May 13) (Apply)
16. Explain the parallel communication interface with the microprocessor.(April/May 2017)(Nov 12)(Apply)
17. Draw the functional block diagram and control word format of 8254 programmable interval timer and its mode of operation and explain. (May 10, May 12)(Create)
18. Explain in detail about 8257 DMA controller with a neat block diagram. (May 11) (May/June 2016) / Explain in detail about DMA controller (Apr/May 2018)(Apply)
19. Explain the four modes of keyboard operation in 8279. (Nov 10)
20. Explain the mode 0 operation of programmable peripheral interface. (May 2014) (Apply)
21. Draw the block diagram and explain the operations of 8251 serial communication interface (Nov/Dec 2015) (Understand)

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- (Create)
22. Draw the block diagram of programmable interrupt controller and explain its operations (Nov/Dec 2015)
- (Create)
23. Explain the different modes of operation of a timer. (May 2014) (May/June 2016)
- (Understand)
24. Explain the internal architecture of 8237 Direct Memory Access controller. (May 2014) (Nov/Dec 2016)(April/May 2017)
- (Understand)
25. Explain the procedure of interfacing D/A and A/D converter circuit. (NOV/DEC 2016)(Apply)
26. Draw the block diagram of the PPI 8255 and explain the ports and modes of the chip. (NOV/DEC 2019)
- (Remember)
27. Write a program in assembly language to set/reset the following bits of Port C. Use the BSR feature of the chip. (NOV/DEC 2019)
- (Understand)
- 1) PC0 to be set
  - 2) PC7 to be reset
  - 3) PC1 to be set
28. Draw the connections between an ADC and 8086, using 8255 as an interface. Write a program to generate a triangular waveform using this setup. (NOV/DEC 2019)(Remember)
29. Draw the block diagram of the 8251 and discuss how it caters to serial communication. Write the steps in transmitting one byte of data serially. (NOV/DEC 2019) (Remember)
30. Draw and explain the functional diagram of 8251 (Nov/Dec 2017)(Remember)
31. Draw and explain the functional diagram of keyboard and display controller (Nov/Dec 2017) (Remember)
32. Draw the block diagram and explain the operations of USART (Apr/May 2018) (Remember)
33. How are D/A and A/D interfaces used ? Explain.(Nov /Dec 2018) (Remember)
34. What are Interrupt controller and DMA controller ? Explain (Nov /Dec 2018) (Remember)
35. Draw the Block diagram and explain the operations of 8251 serial communication interface (Apr / May 2019) (Remember)
36. Explain in detail about interfacing of four LCD digits to 8086 (Apr / May 2019) (Remember)

### PART - C

1. Draw the block diagram of I/O interface & explain in detail
2. Write short notes on
  - (i) LED display
  - (ii) LCD display
  - (iii) Keyboard display interface
3. Develop a 8086 based system to display the word HELLO for every 2ms in the common cathode seven segment LED display and check how many times the word displayed for one hour. (April/May 2017) (Evaluate)
4. Develop a 8086 based system with 128 RAM and 4K ROM, to display the

(Create)  
(Understand)

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word HAPPY for every 2ms in the common anode seven segment LED display. Explain the delay timings. (Nov/Dec 2017)

(Apply)

5. Draw and explain the block diagram of alarm controller. (Apr/May 2018)(Understand)
6. Draw the block diagram of traffic light control system using 8086. Write the algorithm and ALP for traffic light control system. (Apr/May 2018)[Nov/Dec 2021](Understand)



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## UNIT – IV MICROCONTROLLERS

### Part – A

#### 1. What is microcontroller? (Remember)

Microcontroller incorporates all the features that are found in microprocessor with the added features of in-built ROM, RAM, Parallel I/O, Serial I/O, counters and clock circuit to make a micro computer system on its own.

#### 2. What are the alternate functions of Port 3 in 8051 microcontroller?

(Remember)

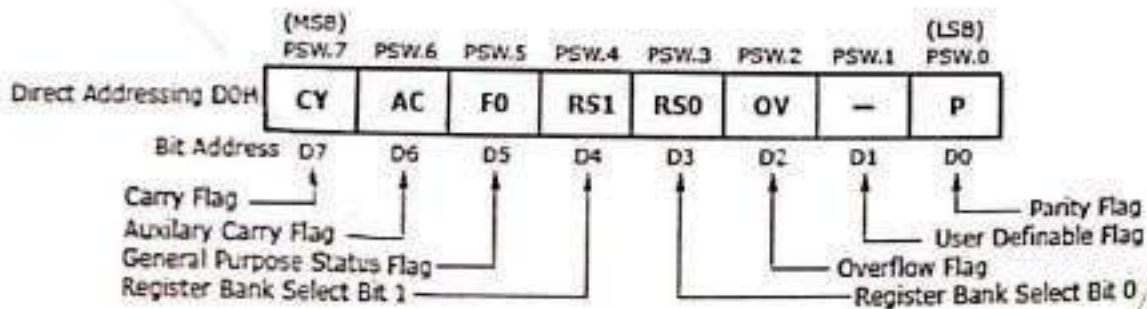
- P3.0-  
RXD
- P3.1-  
TXD
- P3.2-  
INT0
- P3.3-  
INT1
- P3.4-T0
- P3.5-T1
- P3.6-WR
- P3.7-RD

#### 3. What is the function of SM2 bit present in SCON register in 8051?(Remember)

- SM2 enables the multiprocessor communication feature in modes 2 and 3. If SM2 = 1, RI will not be activated if the received 9<sup>th</sup> data bit (RB8) is 0.
- In mode 1, if SM2 = 1, RI will not be activated if a valid stop bit was not received.
- In mode 0, SM2 should be 0.

#### 4. Draw the diagram for processor status word (PSW) in 8051. (Apr/May 2015) [NOV/DEC 2021]

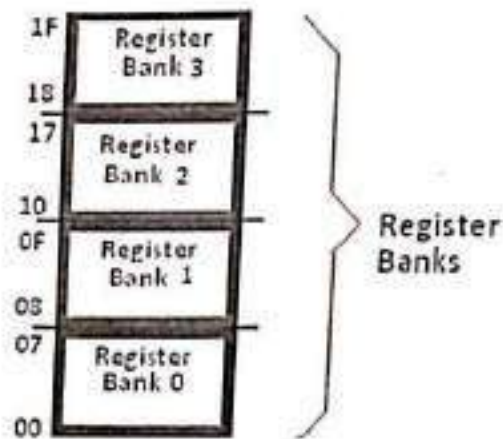
(Understand)



#### 5. How do you select the register bank in 8051 microprocessor?(Apr/May 2015) (Remember)

8051 microprocessor consists of four register banks, such as Bank0, Bank1, Bank2, Bank3 which are selected by the PSW (Program Status Word) register. These register banks are present in the internal ROM memory of the 8051 microcontroller, and are used to process the data when the microcontroller is programmed.

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6. What is the advantage of microcontroller over microprocessor?(Remember)
- The overall system cost is low, as the peripherals are integrated in a single chip.
  - The size is very small
  - The system is easy to troubleshoot and maintain.
  - If required additional RAM, ROM and I/O ports may be interfaced.
  - The system is more reliable.

7. What is the function of IP register in 8051? (Remember)

The IP register is used to set high priority to one or more interrupts in 8051.

-	-	-	PS	PT1	PX1	PT0	PX0
---	---	---	----	-----	-----	-----	-----

Setting a bit to 1 makes the corresponding interrupt to have high priority and setting a bit to 0 makes the corresponding interrupt to have low priority.

8. Define baud rate.(Remember)

Baud rate is used to indicate the rate at which data is being transferred.

Baud rate = 1/Time for a bit cell.

9. If a 12 Mhz crystal is connected with 8051, how much is the time taken for the count in timer 0 to get incremented by one?(Remember)

$$\begin{aligned} \text{Baud rate} &= \text{oscillator frequency}/12 \\ &= (12 \times 10^6) / 12 \\ &= 1 \times 10^6 \text{Hz} \end{aligned}$$

$$\begin{aligned} T &= 1/f \\ &= 1 / (1 \times 10^6) \\ &= 1 \mu \text{ sec} \end{aligned}$$

10. What is the importance of special function registers (SFR) in 8051?

(Remember)

The 8051 operations that do not use the internal 128 byte RAM address from 00 H to 7F H are done by a group of special internal registers called SFRs (Special Function Registers) which have address between 80 H and FF H.

11. Name any 4 additional hardware features available in 8051 when compared to microprocessor.

(Remember)

ROM, RAM, Parallel I/O, Serial I/O, Counters, and a clock circuit are available.

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((SP)) ← (direct)

The SP is incremented by 1. The content of the indicated register is then copied to the internal RAM location addressed by SP.

POP direct: (direct) ← ((SP))  
(SP) ← (SP) - 1

The content of the internal RAM location addressed by SP is read, and SP is decremented by one. The value is then transferred to the directly addressed byte indicated.

19. How does 8051 differentiate between the external and internal program memory?(Remember)

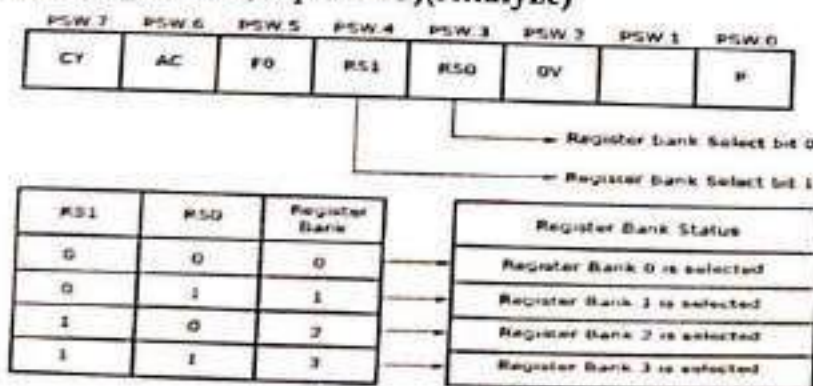
S.N O	EXTERNAL PROGRAM MEMORY	INTERNAL PROGRAM MEMORY
1.	EA pin is high	EA pin is grounded
2.	PSEN signal is activated	PSEN is grounded
3.	8051 can address up to 64 KB of External program memory	4KB of internal program memory is available
4.	Accessible by only direct and indirect addressing modes	Accessible by all addressing modes

20. What are the two memory address pointers in 8051 microcontroller?

(Remember)

Program counter and Data Pointer are the two memory address pointers in 8051. The program instruction bytes are fetched from the locations in memory that are addressed by the PC. The DPTR register is made up of two 8 bit registers named DPH and DPL, which are used to furnish memory address for internal and external code access and external data access.

21. Give the PSW setting for register bank 2 as default bank in 8051 microcontroller.(Apr 2010, Apr 2013)(Analyze)



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22. What is the difference between timer and counter operation in 8051? [NOV/DEC 2021](Remember)

The timer counts the internal clock pulses whose frequency is 1/12<sup>th</sup> of oscillator frequency. The counter counts the internal clock pulses which are given through T0 pin (for counter 0) and T1 pin (for counter 1) of 8051.  
 reliability.

12. What is the function of DPTR register?

The data pointer register (DPTR) is the 16 bit address register that can be used to fetch any 8 bit data from the data memory space. When it is not being used for this purpose, it can be used as two eight bit registers, DPH and DPL.

13. What are the features of 8051 microcontroller?

- 8 bit CPU with registers A and B
- 16 bit PC and DPTR
- 8 bit PSW
- Internal ROM of 4KB
- Internal RAM of 128 bytes
- Two 16 bit timers and counters: T0 and T1
- Two external and three internal interrupts
  - 32 input / output pins arranged as four 8 bit ports: Port0, port1, port2 and port3.
- Control registers are: TMOD, TCON, SCON, PCON, IP and IE.

14. List any applications of microcontroller

- Industrial control (process control)
- Motor speed control (stepper motor control)
- Peripheral devices (printer)
- Stand-alone devices (colour Xerox machine)
- Automobile applications (power steering)
- Home applications (washing machine)
- Length measurement
- Square wave generator

15. What is keydebouncing? (Remember)

When a key press is found, the microcontroller waits for at least 10ms before it accepts the key as input. It is called as key debouncing.

16. What is the maximum frequency of the clock signal that can be counted by 8051 counter? (Remember)

The maximum frequency of the clock signal is  $1/12^{th}$  of the oscillator frequency.

17. Explain the instruction SWAP. (Understand)

SWAP instruction works only on the accumulator (SWAP A). It swaps the lower nibble and higher nibble. The lower 4 bits are put into the higher 4 bits and the higher 4 bits are put into the lower 4 bits.

E.g.- SWAP A

After  
execution:

AC  
C

Before execution:

1111
0000
0000
1111



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18. Explain the PUSH and POP instruction in 8051? (Understand)

PUSH direct:  $(SP) \leftarrow (SP) + 1$

1. Explain the architecture of 8051 microcontroller with neat block diagram.(Nov 07,May 07,Nov 05,Nov 08,Nov 06,May 06, May 08,May 12, May 2015, May/June 2016, NOV/DEC 2016, Nov/Dec 2017, Apr/May 2018)[Nov/Dec 2021](Understand)
2. Draw and explain the pin configuration of 8051.(May 08, Nov 11) (UNDERSTAND)
3. Explain the I/O port structure of 8051. (May 12) (Understand)
4. How a program and data memory is interfaced with 8051?(May 12)(Remember)
5. Briefly explain about 8051 addressing modes.(Understand)
6. Write short notes on instruction set of 8051.(Understand)
7. Discuss about the Special Function Registers (SFRs) of 8051.(Create)
  8. Describe briefly various registers in 8051 microcontroller. (May 11,Nov 11) (Evaluate)
9. Explain the features of 8051 and compare it with 8086. (May 11) (Understand)
10. Describe the functions of signals present in 8051. (May 13)(Evaluate)
11. Draw the pin diagram of 8051 microcontroller and explain the Input / Output lines in detail. (May 14)(Understand)
12. Explain the TMOD function register & its timer modes of operations. (Apr/May 2015)(Understand)
13. Explain about Arithmetic & control instruction set in 8051. (Apr/May 2015)[Nov/Dec 2021] (Understand)
14. Briefly explain about addressing modes of 8051 (Nov/Dec 2015) (APR/MAY 2017)/ Discuss on different addressing modes of 8051 with suitable examples (Apr/May 2018, Apr / May 2019) (Understand)
15. Give PSW of 8051 and describe the use of each bit in PSW (Nov/Dec 2015) (Understand)
16. Describe the functions of the following signals in 8051. RST,EA,PSEN and ALE(Nov/Dec 2015) (Evaluate)
17. Write a program to bring in data in serial form & send it out in parallel form using 8051. (Apr/May 2015) (Understand)
18. Write an 8051 ALP to create a square wave of 66% duty cycle on bit 3 of port1. (May/June 2016) (Understand)
19. Write an ALP using 8051 instructions to receive byte of data serially and put them in PL.Set the baud rate at 4800,8-bit data, 1 stop bit. [NOV/DEC 2016] (Understand)
20. Write the available special function registers in 8051. Explain each register with its format and functions.[APR/MAY 2017] (Understand)

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21. Write an 8051 assembly language program to multiply the given number 48H and 30H. [APR/MAY 2017] (Understand)
22. Write a program for generation of unipolar square waveform of 1 KHZ frequency using Timer 0 of 8051 in mode 0. Consider the system frequency as 12MHZ. [APR/MAY 2017] (Understand)
23. Demonstrate the interfacing of the stepper motor with 8051 and explain its interfacing diagram and develop program to rotate the motor in clock wise direction. [APR/MAY 2017] (Understand)
24. For 8051 microcontroller, discuss the following:
  - i) How is RAM organized and addressed?
  - ii) How many register banks are present in RAM and how is bank switching executed? [NOV/DEC 2019] (Remember)
25. Write a program in 8051 Assembly language to find the biggest of three numbers. [NOV/DEC 2019] (Understand)
26. Write a program in 8051 Assembly language to create a delay of 0.5 seconds, for a clock frequency of 20 MHz. (Note: Do not use any hardware timer) [NOV/DEC 2019] (Understand)
27. Discuss the ports and its circuits of 8051 (Nov/Dec 2017) (Understand)
28. What are special function registers ? explain (Nov/Dec 2015, Nov /Dec 2018) (Understand)
29. How input /output pins and ports help in a circuit of a microcontroller (Nov /Dec 2018) (Understand)
30. i) Explain in detail about the 8051 register banks and stack. (Apr / May 2019) (Understand)
  - ii) Show the code to push R5 R6 and A onto the stack and then pop them back into R2, R3 and B , where register B = register A , R2 = R6 and R3 = R5. (Apr / May 2019) (Understand)
31. Briefly explain about the various addressing modes of 8051 with one example. (Apr / May 2019) (Understand)
32. Write a program to subtract any two 8-bit data using 8051 (Nov/Dec 2021) (Understand)

  
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### Part – C

- Write an 8051ALP to create a square wave 66% duty cycle on bit3 of port 1.  
(Understand)
2. Write a program to bring in data in serial form and send it out in parallel form using 8051.(Understand)
  3. How Microprocessor and microcontrollers are different from computer based controllers? (Nov /Dec 2018) (Understand)
  4. How microprocessor and microcontroller can help to control a process or a machine tool?(Nov /Dec 2018)(Understand)
  5. i) Discuss the number of pin sets aside for addresses in each of the following memory chips (1) 16K x 4 DRAM and (2) 16K x 4 SRAM  
ii) Briefly explain about the interfacing of 8051 with external data ROM.  
(Apr/ May 2019)(Understand)



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# UNIT – V INTERFACING MICROCONTROLLER

## Part – A

1. Name the interrupts of 8051 microcontroller.

(Understand) External interrupt-0, External interrupt-1, Timer-0 interrupt, Timer-1 interrupt, and serial port interrupt

2. What is the job of the TMOD register?

(Understand) TMOD (timer mode) register is used to set the various timer operation modes. TMOD is dedicated to the two timers (Timer0 and Timer1) and can be considered to be two duplicate 4 bit registers, each of which controls the action of one of the timers

3. Differentiate between timers & counters. Draw the diagram of TCON in 8051. (Apr/may 2015)

(Analyze)

The only difference between counting and timing is the source of the clock pulses to the counters.

4. What are the bits available in TMOD register?

(Remember)

GATE	C/T	M1	M0	GATE	C/T	M1	M0
TIMER 1				TIMER 0			

M1	M0	Mode
0	0	0 (13 bit Timer Mode)
0	1	1 (16 bit Timer Mode)
1	0	2 (8 bit auto reload)
1	1	3 (split Timer Mode)

GATE: Gating control when set

C/T : Timer or counter selection; 1 = counter, 0 = Timer.

5. What are the external hardware interrupts in 8051?  
(Remember)

INT0 - External hardware interrupt 0  
INT1 - External hardware interrupt 1

6. What is the interrupt priority in 8051 and write its vector address?(Remember)

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PRIORITY	SEQUENCE INTERRUPTS	ADDRESS
Highest priority	- External interrupt - 0 (INT 0)	- 0003 H
	Timer interrupt - 0	(TF 0) -
	000B H	
	External interrupt - 1 (INT 1)	- 0013 H
	Timer interrupt	- 1 (TF 1)
	-001B H	
Lowest priority	- serial communication (RI, TI)-	0023 H

7. When 8051 is reset, all interrupts are disabled. How to enable these interrupts?

(Remember)

Each of the interrupts sources can be individually enabled or disabled by setting or clearing a bit in the Special Function Register IE. IE also has a global disable bit, which disables all interrupts at once.

8. What is nested interrupts?

(Remember) The 8051 is executing an ISR for servicing an interrupt and another interrupt occurs. If the new coming interrupt is high priority then only it can interrupt the previously occurred low priority interrupt. These are called nested interrupts.

9. Give steps to program 8051 for serial data transfer.

(Understand) The 8051 has a serial data communication circuit that uses register SBUF to hold data. Register SCON controls data communication, register PCON controls data rates, and pins RXD (P3.0) and TXD (P3.1) connect to serial data network.

10. What is the significant of GATE in TMOD control register?

(Remember)

It is OR gate enable bit which controls RUN/STOP of timer 1/0. Timer/ Counter is enabled while TR 1/0 in TCON is set and signal on external interrupt INT1/0 pin is high. Cleared to 0 by program to enable timer to run, if bit TR1/0 in TCON is set.

11. List the I/O ports available in 8051. (Remember)

Port0, Port1, Port2, Port3

12. Write down the different operating modes for serial

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**communication of 8051.**

**(Remember)**

Serial communication of 8051 operates under four modes. They are mode 0, mode 1, mode 2 and mode 3. SM0 and SM1 bits of SCON register specifies the mode.

**13. What are the timers available in 8051?**

**(Remember)**

- Timer 0, Timer 1

Each 16 bit timer is accessed as two separate 8 bit registers: Low byte register (TL) and High byte register (TH).

**14. Compare polling and interrupt. (May/June 2016)**  
**(Understand)**

In the Polling method, the microcontroller must "access by himself" the device and "ask" for the information it needs for processing. In fact we see that in the Polling method the external devices are not independent systems; they depend on the microcontroller, and only the micro is entitled to obtain access to the information it needs.

Interrupt is the signal sent to the micro to mark the event that requires immediate attention. Interrupt is "requesting" the processor to stop to perform the current program and to "make time" to execute a special code. Whenever any device needs its service, the device notifies the microcontroller by sending it an interrupt signal. Upon receiving an interrupt signal, the microcontroller interrupts whatever it is doing and serves the device.

**15. Define baud rate of 8051. (May/June 2016)**  
**(Remember)**

The 8051 transfers and receives data serially at many different baud rates. The baud rate in 8051 are completely programmable. This is done with help of timer 1.

**16. Mention the features of serial port in mode 0**  
**(Nov/Dec 2015) (Remember)**

In mode 0, the baud rate is always the oscillator frequency divided by 12. This means if you're crystal is 11.059 Mhz, mode 0 baud rate will always be 921,583 baud.

**17. List the modes of Timer in 8051.**  
**[NOC/DEC 2016]. (Remember)**

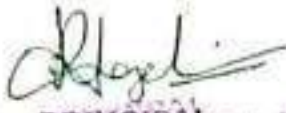
Mode 0- 13-bit Timer

Mode 1- 16-bit

Timer Mode 2-

8-bit Auto reload

Mode 3- Splitter Timer mode

  
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18. List the 8051 interrupts with its priority.[APR/MAY 2017, Nov/Dec 2017]/Give the priority level of the interrupt sources in 8051 (Apr/May 2018) (Remember)

Timer 0 overflow interrupt-

TF0 Timer 1 overflow

interrupt- TF1 External

hardware interrupt- INT0

External hardware interrupt-

INT1

Serial communication interrupt- RI/TI

19. What are the types of sensors used for interfacing? [APR/MAY 2017, Apr/May 2018] (Remember)

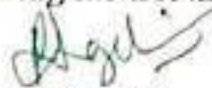
Temperature Sensor, IR Sensor, Ultrasonic Sensor, Touch Sensor, Proximity Sensors, Pressure Sensor, Level Sensors, Smoke and Gas Sensors.

20. Give the format and list the function of the instruction DJNZ for 8051. (NOV/DEC 2019)(Remember)

**Function:** Decrement and Jump if Not Zero

**Syntax:** DJNZ register,reladdr

DJNZ decrements the value of *register* by 1. If the initial value of *register* is 0, decrementing the value will cause it to reset to 255 (0xFF Hex). If the new value of *register* is not 0 the program will branch to the address indicated by *relative addr*. If the new value of *register* is 0 program flow continues with the instruction following the DJNZ instruction.



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### Part - B

1. Describe the different modes of operation of timers/counters in 8051 with its associated register.(Apr/May 2015)(Evaluate)
2. How does one interface a 16 X 2 LCD display using 8051 microcontroller? (Apr/May 2015) (Remember)
3. Explain the interfacing of DAC with 8051 with neat block diagram. (May 11, May 13)(Understand)
4. Write an 8051 assembly language program to transfer the letter 'A' serially with 4800 baud, 1stop bit continuously.(Understand)
5. Explain the on-chip timer modes of 8051.(May 10)(Understand)
6. How to transfer data between a PC and microcontroller using serial communication?(Remember)
7. Draw the necessary diagrams and explain. (Nov 12)(Understand)
8. What is timer/counter? Explain 16-bit timer mode and 8-bit auto reload mode of 8051. (Nov 12)(Remember)
9. Explain how LCD and keyboard is interfaced with 8051.(May 13) (Understand)
10. Describe about serial port interface of 8051.(May 13) (May/June 2016)(Remember)
11. Explain the different techniques to convert a digital quantity into its equivalent analog quantity. (May 2014)(Understand)
12. With a neat circuit diagram explain how a 4 x 4 keypad is interfaced with 8051 microcontroller and write 8051 ALP for keypad scanning. (Nov/Dec 2015)(Remember)
13. Draw the schematic for interfacing a stepper motor with 8051 microcontroller and write ALP for changing speed and direction of motor (Nov/Dec 2015)(Understand)
14. Draw the diagram to interface a stepper motor with 8051 microcontroller & explain. Write a 8051 assembly language program to run the stepper motor in both forward & reverse direction with delay. (Apr/May 2015) (May/June 2016)(Understand)
15. Describe the different modes of operation of timer/counter in 8051 microcontroller. [NOV/DEC 2016]/ Describe the different modes of operation of timer/counters in 8051 with its associated registers (Apr/May 2018)(Remember)
16. Draw a diagram to interface a stepper motor with 8051 microcontroller and also write an 8051 ALP to run the stepper motor in both forward and reverse direction with address.[NOV/DEC 2016]. (Understand)
17. Write a program for generation of unipolar square waveform of 1 KHZ frequency using Timer 0 of 8051 in mode 0. Consider the

system frequency as 12MHz. [APR/MAY 2017].

(Understand)

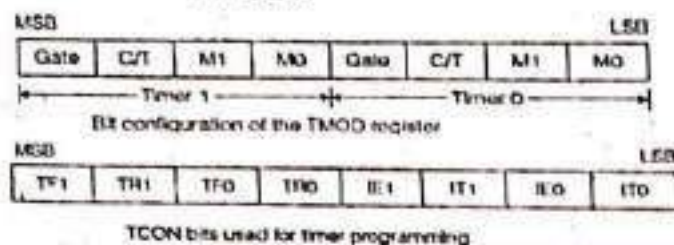
18. Demonstrate the interfacing of the stepper motor with 8051 and explain its interfacing diagram and develop program to rotate the motor in clock wise direction. [APR/MAY 2017].

(Understand)

19. Draw and explain the interfacing connections between an 8051 and a stepper motor by using driver IC as an interface. Write the steps and assembly program to rotate the stepper motor in the clockwise direction. [NOV/DEC 2019]. (Understand)

20. i) Write the assembly language program to generate a square wave using any timer, for an 8051 microcontroller.[NOV/DEC 2019].(Understand)

ii) For the above generated square wave, if the crystal frequency is 20 MHz and the frequency of the wave is 10KHz. Write the assembly language program referring to the bit configuration given below: [NOV/DEC 2019] (Apply)



21. Illustrate the serial communication in 8051 with its special function register. (Nov/Dec 2017)(Understand)

22. i) Interface the ADC converter with 8051 and explain with neat diagram. (Nov/Dec 2017)(Understand)

ii) Write the assembly language program to execute the ADC conversion.

(Nov/Dec 2017)(Apply)

23. Draw the diagram to interface a stepper motor with 8051 microcontroller and write an ALP to run the stepper motor in both forward and reverse direction with delay. (Apr/May 2018)[Nov/Dec 2021](Apply)

24. Write and explain what is known as serial port programming (Nov/Dec 2018) (Understand)

25. What are sensor interfacing and external memory interfacing? Explain (Nov /Dec 2018) (Understand)

26. Describe how to program and interface an LCD to an 8051 using Assembly Language Programming (Apr / May 2019)

(Apply)

27. Draw and explain the DAC interfacing using 8051(Apr/May 2019)(Understand)

28. Write a program to display a character using LCD

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display[Nov/Dec 2021]

Part – C

1. Explain about external memory interfacing to 8051  
(Evaluate)
2. Draw and explain the ADC and DAC interfacing using 8051 (Understand)
3. Develop 8051 based system design having 8Kbyte RAM to generate the triangular wave using DAC. (APR/MAY 2017). (Create)
4. Design a microcontroller based system for taking sensor data from an agricultural field and displaying the data, generating alarms, causing actuations and also for sending the data to a PC. A complete description of this system could be given.

The following points are to be taken care of.

- i) Draw a block diagram of the system and suggest a suitable microcontroller.
- ii) Humidity and temperature are the sensor data
- iii) Show the device that displays these parameters
- iv) If these sensor values go above a threshold, sound alarm and display should occur.
- v) If temperature goes above a threshold, a motorized pump should be activated to water the field.
- vi) Enumerate the steps for the microcontroller to be connected to the P.C

[NOV/DEC 2019]

(Create)

5. With neat block diagram explain the functions of ARM processor. Compare it with PIC and list out the major differences. [NOV/DEC 2019](Understand)
6. Design a circuit to generate 12MHZ frequency for a system. Write a program for generation of unipolar square waveform of 1KHz frequency using Timer 0 of 8051 in mode 0.(Nov/Dec 2017) (Apply)
7. i) Discuss what happens if interrupts INTO, TFO and INT1 are activated at the same time. Assume priority levels were set by the power up reset and that the external hardware interrupts are edge triggered.  
ii) With necessary diagrams explain how to interface LM35 temperature sensor and then discuss the issues of signal conditioning(Apr / May 2019)(Under



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# Assignment - 1

Micro Processor  
And  
Micro Controller

Assembler Directives  
of 8086

10

Submitted by,  
R. Santhiya  
III ECE  
20RECL05

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## Assembler Directives

An assembler is a program used to convert an assembly language program into the equivalent machine code modules which may further be converted into executable codes.

Some directives such as `ORG`, `EQU`, `DB`, `DW`, etc. which are common in different assemblers were also described. Though a representative set of directives on the 8086 assembler is presented it is possible that some assemblers have a few additional directives. On the other hand, some of the directives presented here may not be present or may be present in different forms.

### Directives for Constant and Variable Definition

An Intel 8086 assembly program uses different types of constants like binary, decimal, octal and hexadecimal. These can be represented in the program using different suffixes like `B` (for binary), `D` (for decimal), `O` (for octal) and `H` (for hexadecimal) to the constant.

10H is a hexadecimal number

270 is an octal number.

10100B is a binary number.

A number of directives are used to define and store different kinds of constants.

The Define byte, Define word, Define Double word.

The 8086 assembler uses DD as directive for double word.

\* DB : Define Double word

\* DT : Define Ten bytes.

## DUP

Using the DUP directive, several locations may be initialized and the values may be put in those locations. The format is as follows: Name Type Num

Example: TEMP DB 20 DUP(5)

The directive define an array of 20 bytes in memory and each location is initialized to 5. The array is named TEMP. ✓



## ESU

The EQU directive may be used to define a data name with immediate value or another data name. It can also be used to equate a name to a string.

Example: NUMB EQU 20H

NAME EQU "RASHMI"

## Program Location Control Directives

The directives used for program location control in the 8086 assembler are (ORG, EVEN, ALIGN and LABEL).

## ORG

The ORG directive is used to set the location counter to a particular value.

\* ORG 2375H

The location counter is set to 2375H. If it occurs in data segment the next data storage will start at 2375H. If it is in code segment the next instruction will start at 2375H.

## EVEN

Using EVEN directive, the next data item label is made to start at the even address boundary. The assembler on encountering EVEN directive will advance the location counter to even address boundary.

### \* EVEN TABLE DW 20 DUP(0)

This statement declares an array named TABLE of 20 words starting for the even address.

### ALIGN number

This directive will force the assembler to align the next segment to an address that is divisible by 2, 4, 8, or 16. The unused bytes are

### \* ALIGN 2

It will force the next segment to the next even address.

### LENGTH

It is an operator which is used to tell the assembler to determine the number of elements in a data item, such as string or array.

MOV AX, OFFSET FACT

This statement will place in the AX register the offset of the variable FACT from the start of the segment.

OFFSET

This operator is used to determine through the assembler the offset of a data item from the start of the segment containing.

Example: MOV AX, OFFSET FACT

This statement will place in AX register the offset of the variable FACT from the start of the segment.

LABEL

The LABEL directive is used to assign a name to the current value in the location counter. The location counter denoted is used by the assembler to keep track of the current location. The value in the location counter denotes the distance of the current location.

## Segment Declaration Directives.

These directives help in declaring various segments with specific names. The start and the end of segments may also be specified using this directive. The directives for segment declaration include SEGMENT, ENDS, ASSUME, GROUP, CODE, DATA, STACK etc.

### SEGMENT and ENDS.

The SEGMENT and ENDS directives signify the start and end of a segment.

INST SEGMENT

ASSUME CS : INST, DS : DATA W.

\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

INST ENDS ASSUME

The directive is used to assign logical segment to physical segment at any time.

Example: ASSUME : CODE, DS : DATA, SS : STACK

This directive tells the assembler that the CS register will store the address of the segment whose name is CODE and so on.

`.CODE (Name)` .

This code directive is the shortcut used in the definition of code segments. The name is optional and is specified if there is more than one code segment in the program.

`.DATA` and `.STACK` .

Similar to `.CODE` the `.DATA` and `.STACK` directives are shortcuts in the definition of data segment and stack segment, respectively.

`GROUP` .

This device is used to tell the assembler to group all the segments in one logical group segment. This allows the contents of all the segments to be accessed from the same segment base.

Eg: `PROG GROUP CODE , DATA`

The above statement will group the two segment `CODE` and `DATA` into one segment named `PROG`. Each segment must be declared using `ASSUME` statement

`ASSUME CS : PROG DS : PROG`

## Procedure and Macro-related Directives.

The directives in this group relate to the declaration of procedures and macros along with the variables contained in them. The directives include PROC, ENDP, PUBLIC, MACRO, ENDM and EXTRN.

### PROC and ENDP.

The PROC directive is used to define the procedures. The procedure name is a must and it must follow the naming convention of the assembler.

The ENDP directive is used to mark the end of the procedure. Some examples.

```
FUNCT PROC FAR
```

```
====
```

```
ENDP
```

```
FAC1 PROC NEAR
```

```
====
```

```
ENDP
```

The first procedure FUNCT is in a segment which is different from where it is called. The

second procedure, FACT is in the same segment where it is called. All the statements of the procedure are between PROC and ENDP directives. PUBLIC.

It is very much possible that a variable is defined in one module but is used in other modules. In order to facilitate the linking, such variables are declared public, using the PUBLIC directive in the module.

PUBLIC PX, PY, PZ.

### MACRO and ENDM

The MACRO directive is used to define macros in the program. The ENDM directive defines the end of MACRO.

### Other Directives

These directives are of general nature, or they relate to more than one group described earlier. The PTR, PAGE, TITLE, NAME and END.

### PTR.

The PTR is an operator used in instructions to assign a specific type to a variable or a label. The PTR operator can also be used to override the

declared type of variable.

```
ARRAY DW 0125H, 1630H, 9275H, ...
```

In the above array of words, suppose we wish to move a byte from the array, we may then simply insert the PTR operator.

```
MOV AL, BYTE PTR ARRAY.
```

**PAGE :**

The directive is used for listing of the assembled program. At the start of the program, the directive is placed to specify the maximum number of lines on a page and the maximum number of characters.

```
PAGE 60,120.
```

The above example specifies that 60 lines are to be listed on a page with a maximum of 120 characters in each line.



## TITLE

This directive is also used for the listing of the program. The title obtained in this directive defines the title of the program and is listed in line 2 of each page of program listing.

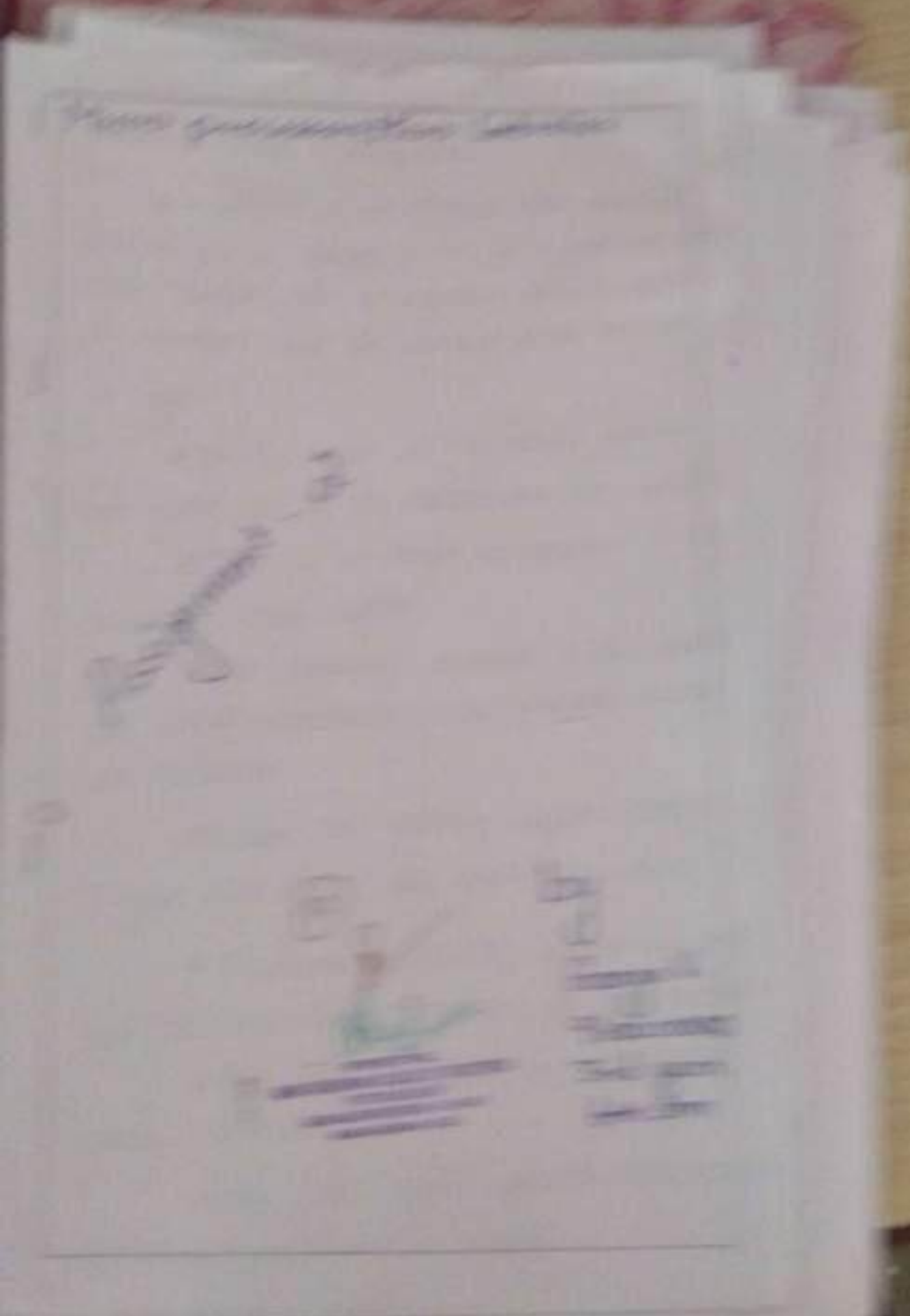
eg. TITLE PROGRAM TO FIND SQUARE ROOT

## NAME

The NAME directive is used to assign a specific name to each module, when the program consists of a number of modules. This helps in understanding the program logic.

## END

This is the last statement of the program and it specifies the end of the program user assembler. It must be noted that not all of the above directives are used in all program. User may deploy them depending on the need of the program logic.



# Micro processor & Micro Controller

Assignment - 2

10



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by.

Gianga V.

9602010602

3rd year,  
6th Sem

## Minimum Mode Configuration :-

\* A processor is in minimum mode when its  $\overline{MN}/\overline{MX}$  pin is strapped to +5V. In a minimum mode 8086 system, the microprocessor 8086 is operated in minimum mode by strapping its  $\overline{MN}/\overline{MX}$  pin to logic 1.

\* In this mode, all the control signals are given out by the microprocessor chip itself.

\* There is a single microprocessor in the minimum mode system.

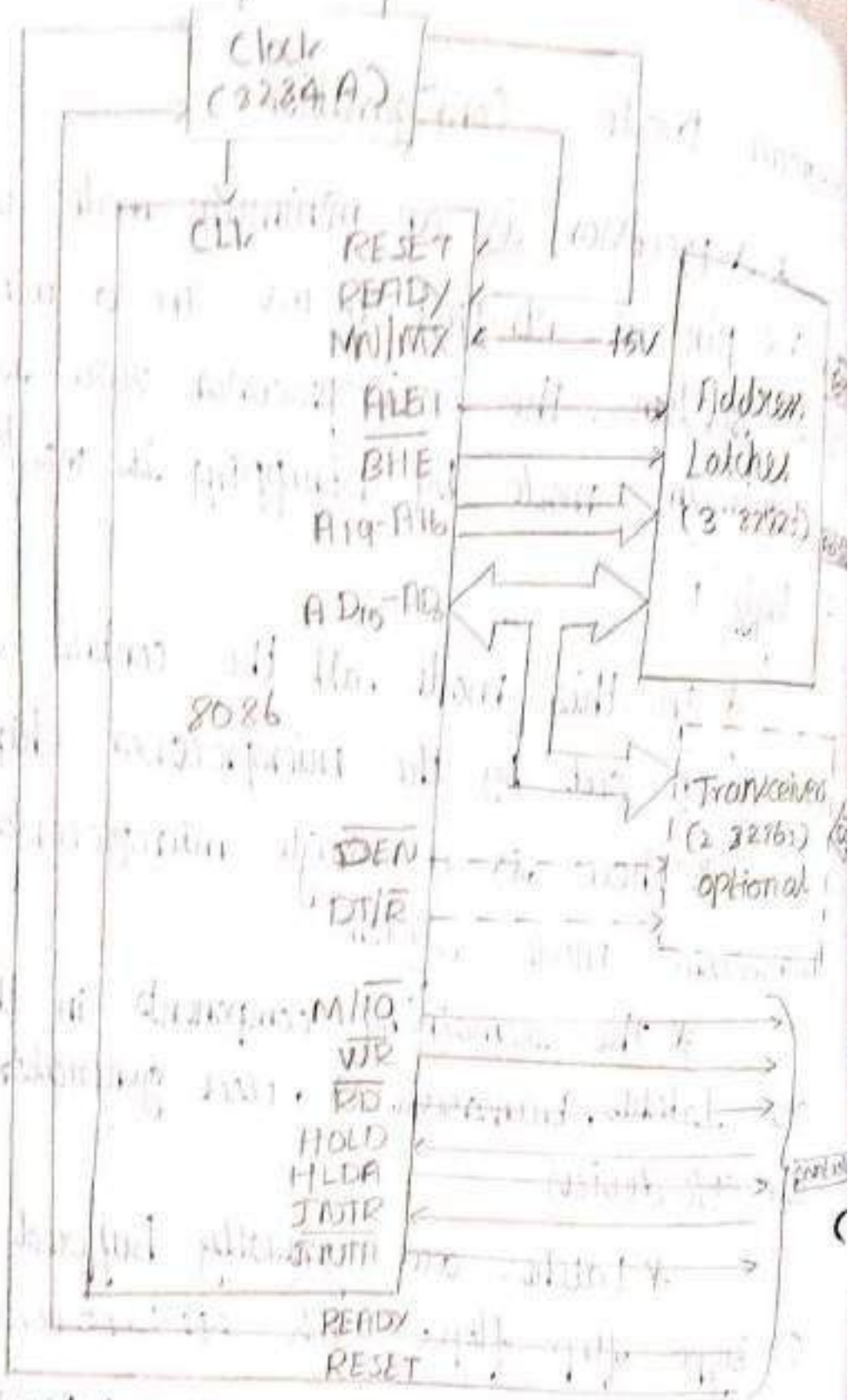
\* The remaining components in the system are latches, transreceivers, clock generator, memory and I/O devices.

\* Latches are generally buffered output D-type flip flops like 74LS373 (or) 8289.

\* Transreceivers are the bidirectional buffers and some times they are called as data amplifiers.

\* They are controlled by two signals namely,  $\overline{DEN}$  and  $\overline{DT/R}$ .

\* The  $\overline{DEN}$  signal indicates the direction of data i.e. from (or) to the processor.



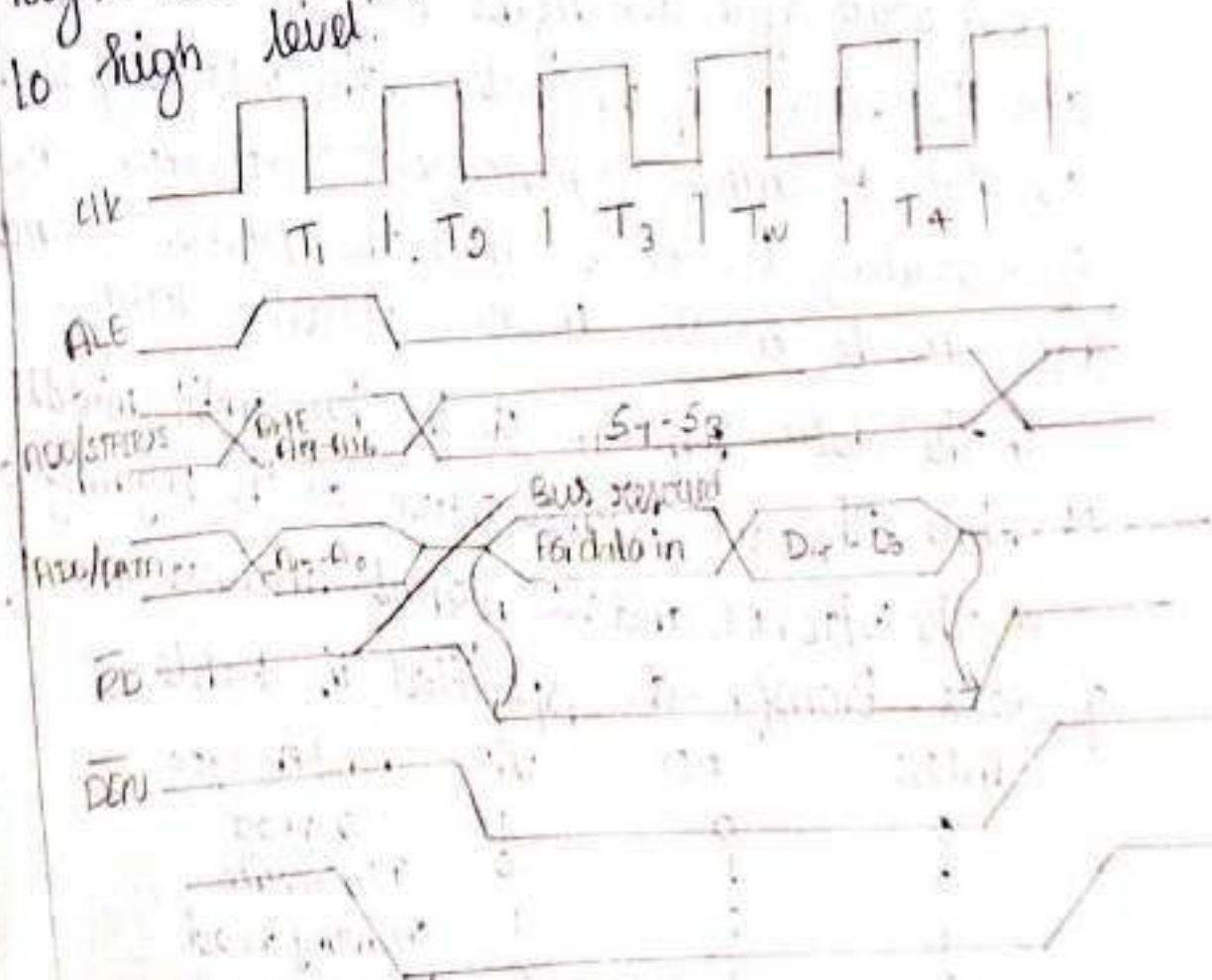
**Bus Timing for Minimum Mode :-**

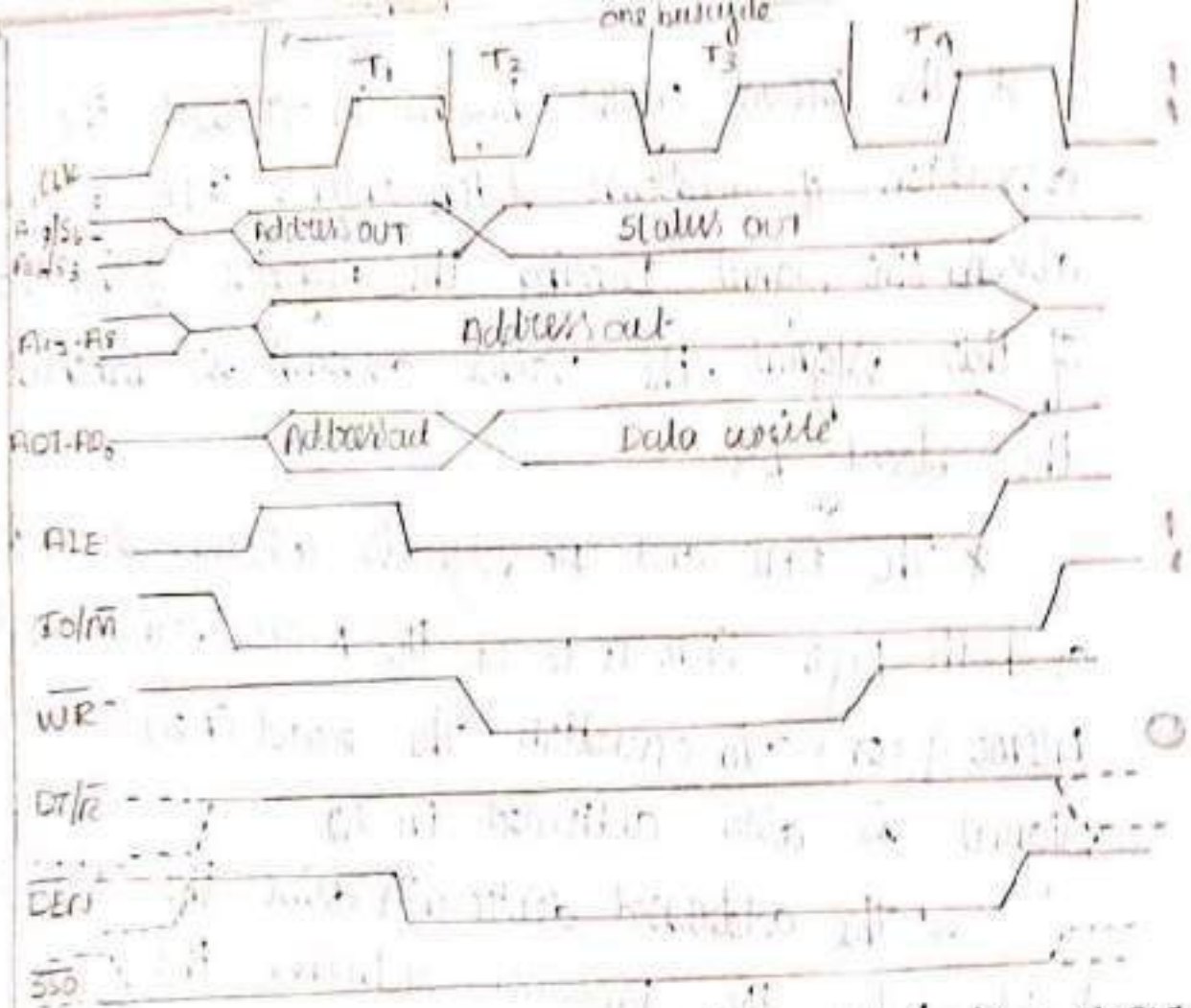
\* The opcode fetch and read cycles are similar. Hence the timing diagram can be categorized in two parts, the first is the timing diagram for read cycle and the second is the timing diagram for write cycle.

\* The second cycle begins in  $T_1$  with the assertion of address latch enable (ALE) signal and also M/IO signal. During the negative going edge of this signal, the valid address is latched on the local bus.

\* The BHE and A0 signals address low, high or both bytes. From  $T_1$  to  $T_4$ , the M/IO signal indicates memory (or) I/O operation. The read (RD) control signal is also activated in  $T_2$ .

\* The addressed device will drive the READY line high. When the processor returns the read signal to high level.





\* A write cycle also begins with the assertion of ALE and the emission of the address. The  $\overline{IO/\overline{M}}$  signal is again asserted to indicate a memory or I/O operation. In  $T_1$ , after sending the address in  $T_1$ , the processor sends the data to be written to the addressed location.

\* The data remains on the bus until middle of  $T_4$  state. The  $\overline{WR}$  becomes active at the beginning of  $T_2$ .

\* The  $\overline{IO/\overline{M}}$ ,  $\overline{RD}$  and  $\overline{WR}$  signals indicate the type of data transfer as specified in table.

$\overline{IO/\overline{M}}$	$\overline{RD}$	$\overline{WR}$	Transfer Type
0	0	1	I/O read
0	1	0	I/O write
1	0	1	memory read
1	1	0	memory write

Micro Processor &  
Micro Controller

Assignment - 3




⑩

by.

Gianga Devi M.

960120106003

3rd year 6th sem



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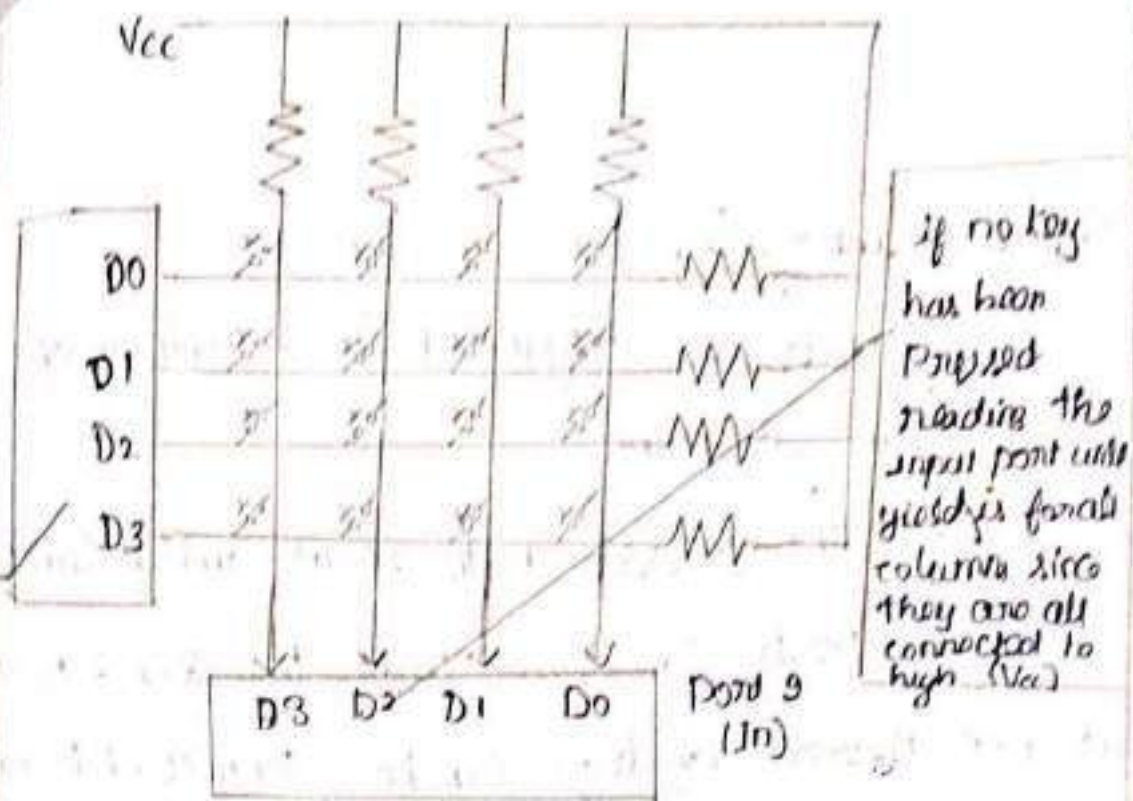
If one of the column bits has a zero, this means that a key press has occurred. For example, if  $D_3-D_0 = 1101$ , this means that a key in the  $D_1$  column has been pressed.

After detecting a key press, microcontroller will go through the process of identifying the key starting with the top row, the microcontroller grounds it by providing a low to row  $D_0$  only.

it reads the columns. if the data read is all 1s, no key is pressed. The row is activated and process is moved to the next row.

it grounds the next row, reads the columns, and checks for any zero.

Find out which column the pressed key belongs to.



it is the function of the microcontroller to scan the keyboard continuously to detect and identify the key pressed. To detect a pressed key, the microcontroller grounds all rows by providing 0 to the output later, then it reads the columns.

if the data read from columns is  $D3-D0 = 1111$ , no key has been pressed and the process continues till key press is detected.

if one of the column bits has a zero, this means that a key press has occurred.

## Keyboard interfacing

Keyboards are organized in a matrix of rows and columns.

The CPU accesses both rows and columns through ports. Therefore, with two 8-bit ports, an  $8 \times 8$  matrix of keys can be connected to a microprocessor.

When a key is pressed, a row and a column make a contact, otherwise, there is no connection between rows and columns.

In IBM PC keyboards, a single microcontroller takes care of hardware and software interfacing. A  $4 \times 4$  matrix connected to two ports.

The rows are connected to two output ports. The columns are to an input port.

KEYBOARD.

Micro Processor &  
Micro Controller

Assignment - A

 10

by.

Sarithiya R.  
960120106005  
3rd year 6th sem



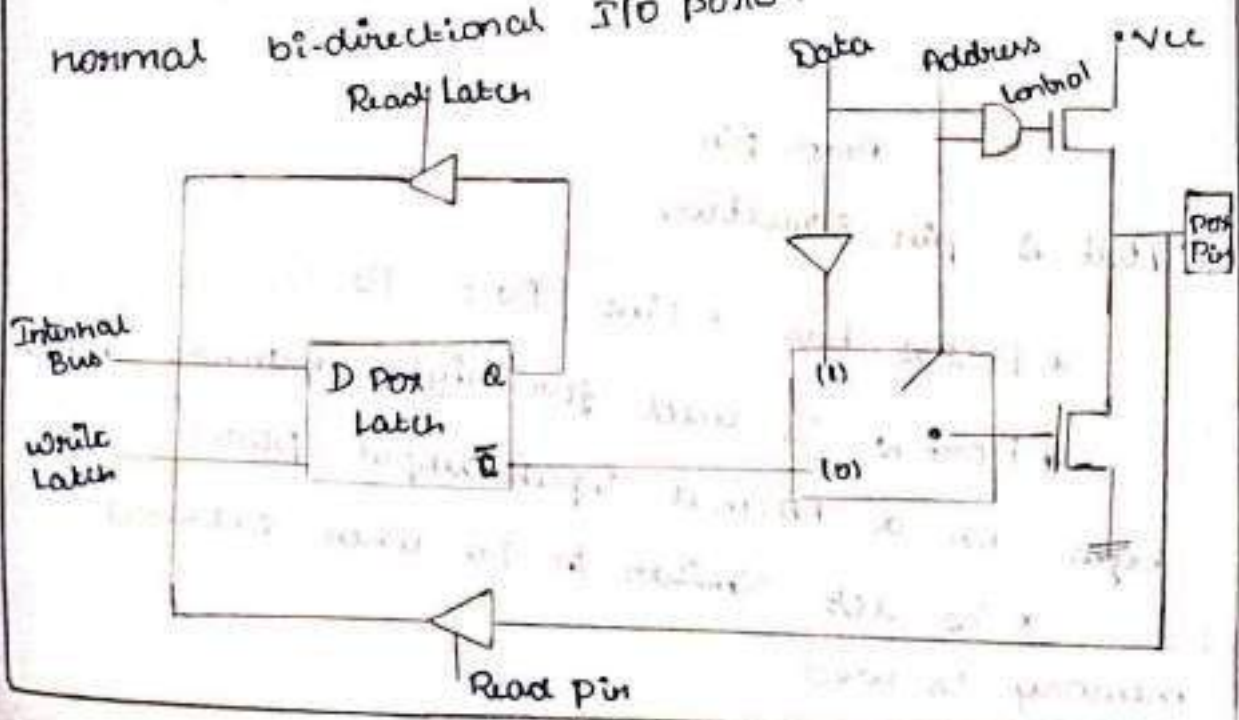
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# I/O ports Pins, and Circuits

- \* 8051 microcontroller has 4 I/O ports.
- Each port has 8 bits which can be used as Input / Output port. Total 32 I/O pins are available.
- \* Each port has bi-directional capacity.

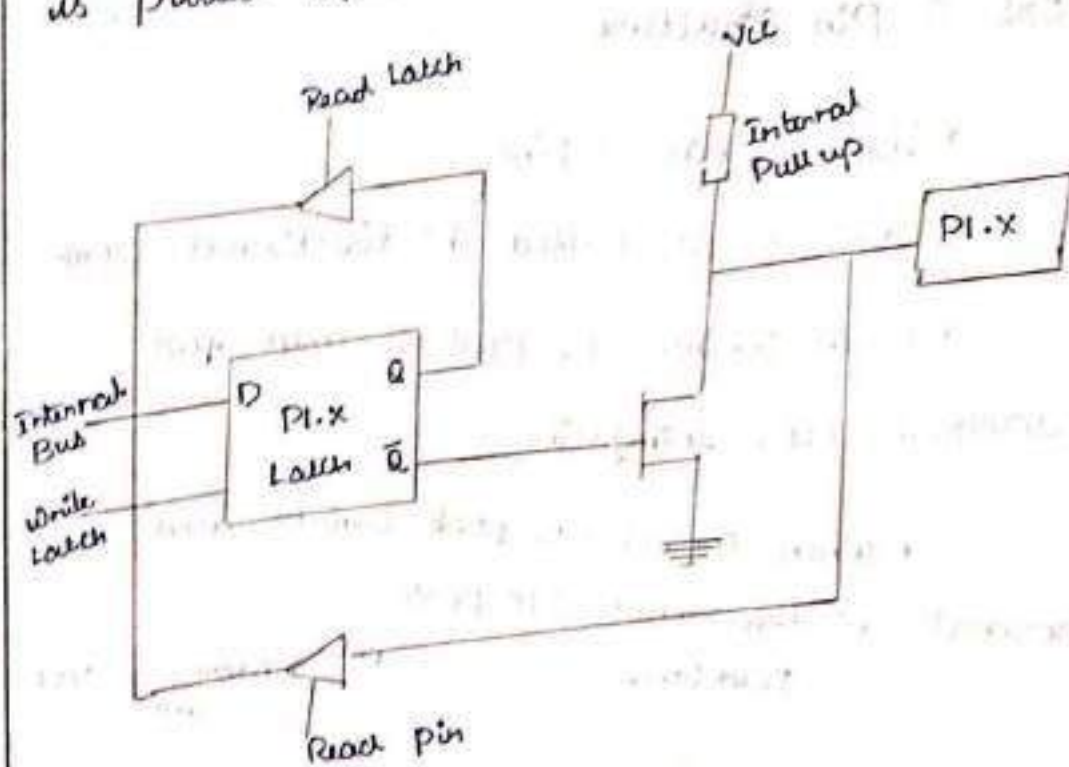
## Port - 0 - Pin structure

- \* Port 0 has 8 pins
- \* Port 0 is called bi-directional port
- \* When control = 1, port is used for address/data interfacing.
- \* When control = 0, port can be used as normal bi-directional I/O port.



## Port - 1 Pin Structure

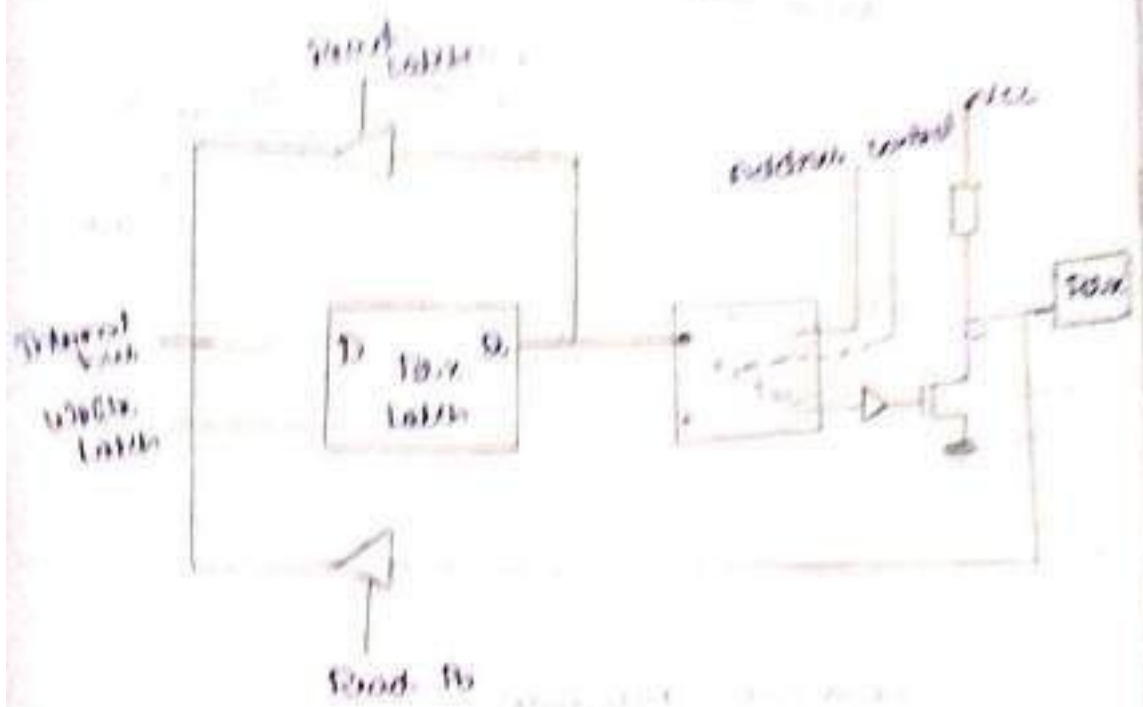
- \* Port 1 has 8 pins (P1.0 - P1.7)
- \* P1 is a true I/O port, because it doesn't have any alternative functions.
- \* It has a pull-up resistor built-in.
- \* When used as output port, the pin is pulled up (or) down.



## Port - 2 pin structure

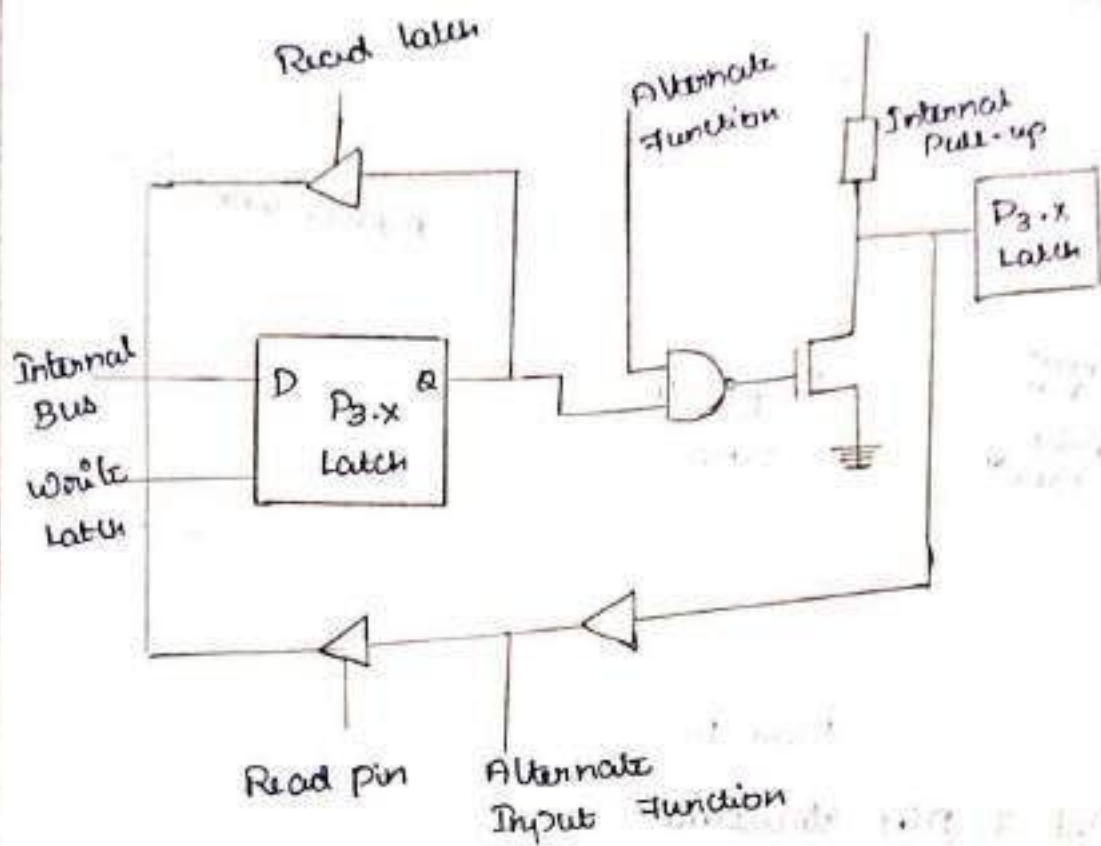
- \* Port 2 has 8 pins (P2.0 - P2.7)
- \* Port 2 is used for higher external address byte on a normal input/output port.
- \* P2 acts similar to P0 when external memory is used.

\* When no memory is available the port can be used as general I/O port.



Port 3 pin structure

- \* Port 3 has 8 pins (P3.0 - P3.7)
- \* Port 3 pins have alternate functions.
- \* All ports can be used as general I/O also they have alternate function.
- \* To use the port as input port it should be written to the latch.



Alternate Functions:

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
RD	WR	T <sub>1</sub>	T <sub>0</sub>	INT1	INT0	TXD	RxD



MICROPROCESSOR AND  
MICROCONTROLLER

ASSIGNMENT - 5

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✓

*[Signature]*  
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C. Sathesh Kumar  
960120106306  
III ECE

## Stepper motor interfacing with 8051

### Micro controller

This is basically a high voltage, high current Darlington transistor array. It has ULN2003 is used and each ULN2003 has seven NPN Darlington Pairs. It can provide high voltage output with common cathode clamp diodes for switching inductive loads.

### Stepper motor Interfacing

Stepper motor is a Brushless DC electric motor that divides the complete rotation into very small angles called steps, usually each step moves 1.8 degree and therefore a total of

200 steps for a rotor  
finish a single rotation. Unlike  
normal DC-motors, it contains  
multiple stator magnets used to  
trigger each step. Also each  
stepper motor will have some  
fixed step angle and also  
the motor rotates at this  
angle.

### Stepper motor

The stepper motors are  
widely used in industrial and  
commercial applications also they  
are also commonly used as in  
drive system of autonomous  
robots.

## Unipolar Steppermotor

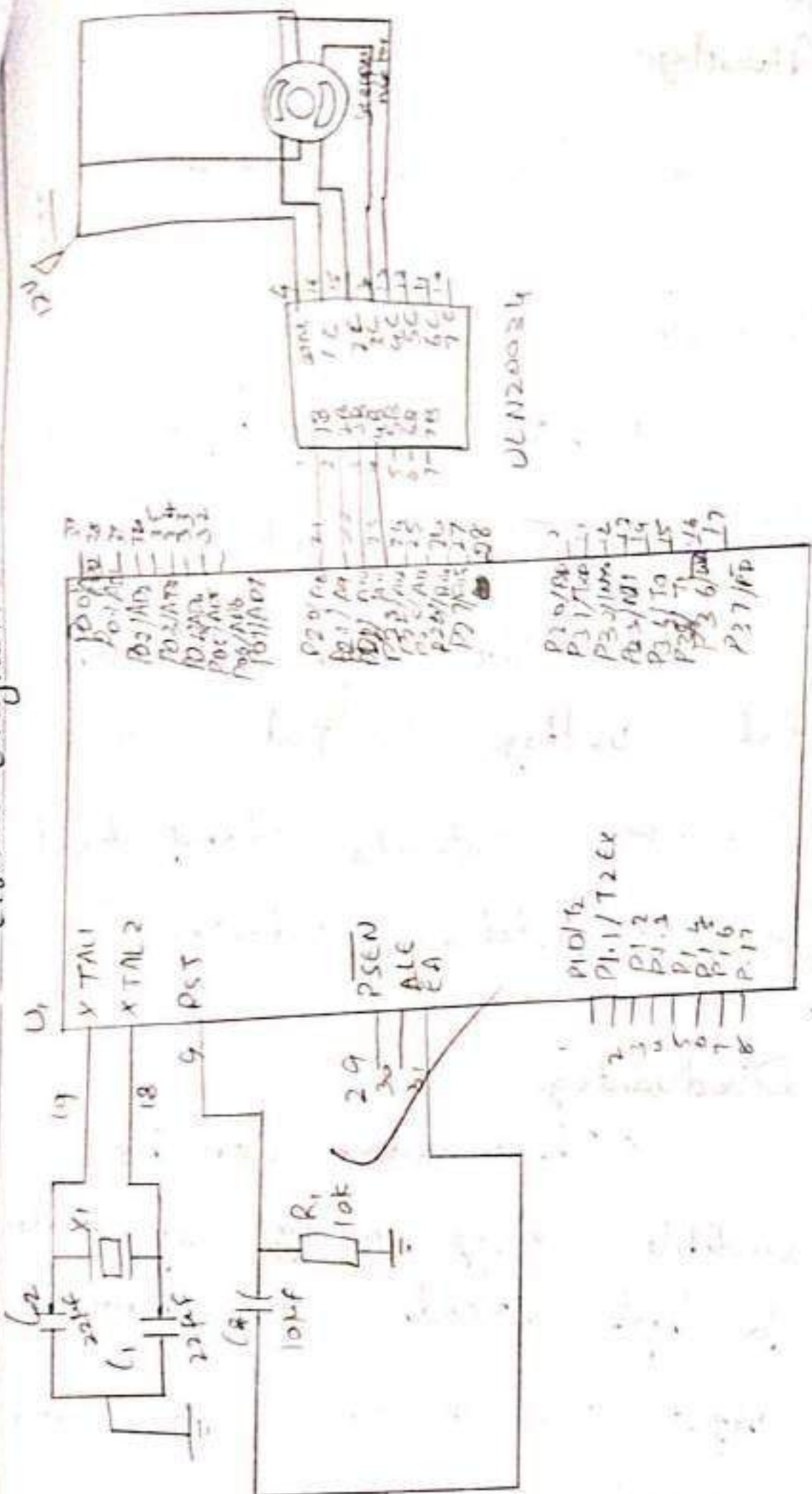
A two phase unipolar Stepper motor has a total of six wires / leads of which four are each wires connected to coils. Stepper motor used here is green. Each common wire is connected to two end leads thus forming two phases. The end leads corresponding to each phase. Also these motors leads in a sequence is sufficient to drive the motor.

# Diagram of wave drive

## Stepper motor

Signal	Sequence	for wave drive	Stepping mode
Step	Yellow	Blue	White
	load	load	load
1	1	0	0
2	0	0	0
3	0	1	0
4	0	0	1

# Circuit Diagram



## Advantage.

\* This is basically in a high voltage.  
\* It has high current  
Darlington transistor array  
\* It can provide high voltage output with common cathode clamp diodes for switching inductive load.

## Disadvantage.

\* These motor can be audible very noisy at moderate to high speeds and have low output power for size and weight.

College Code / Name : 9601 - ANNAI VAILANKANNI COLLEGE OF ENGINEERING

Branch Code / Name : 103 - B.E. Civil Engineering

Semester : 04

University : AUC

Regulation : 2021

S.No	Register Number	Name	CE3401	CE3402	CE3403	CE3404	CE3405	CE3411	CE3412	CE3413	GE3451	NCCXX1	SB8024	SB8025	SB8026
1	960121103001	ABISH R	28	29	28	29	29	57	54	54	29	90			95
2	960121103002	ANU DHARSHINI N	34	34	30	33	32	58	59	58	33				95
3	960121103003	BAVI K	35	36	33	32	35	58	59	58	33				96
4	960121103004	DEVI S	33	34	31	34	33	59	59	57	34				96
5	960121103005	JESHIKA S	34	36	30	33	30	58	56	55	32				96
6	960121103008	PAVITHRA K	34	35	32	33	35	58	58	58	33				99
7	960121103009	SNEKA N	28	28	29	29	28	54	54	54	28				94
8	960121103010	SUBISHA J	29	30	30	30	29	55	54	54	30				96
9	960121103011	SWETHA S	29	29	30	29	28	54	55	54	28	94			96
10	960121103302	ESAKKI PANDI K	30	28	28	30	28	52	53	53	30				
11	960121103305	MAGESH M	30	28	28	29	29	53	53	53	28				
12	960121103306	MARIA AJITH M	30	28	28	28	29	52	54	52	30				
13	960121103307	NIBIN N	29	28	29	28	28	52	53	52	28				
14	960121103308	RATHEESH C	30	30	28	29	29	54	54	52	30				
15	960121103310	SENTHIL KUMAR K	31	30	29	29	30	54	54	52	29				
16	960121103311	SUJIN P	30	28	28	29	28	53	53	52	28				
17	960121103312	VINU C	32	30	29	29	29	52	54	52	30				





Reg. No.

A U H I P P O . C O M \*



Question Paper Code : 27203

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Fourth/Fifth Semester

Computer Science and Engineering

EC 6504 — MICROPROCESSOR AND MICROCONTROLLER

(Common to Information Technology and Medical Electronics/Bio Medical Engineering/Electronics and Communication Engineering)

(Regulations 2013)

Time : Three hours

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Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Calculate the physical address, when segment address is 1085 H and effective address is 4537 H.
2. Show how the 2 byte INT instruction can be applied for debugging.
3. What is multi programming?
4. Schematically show, how synchronization is made between 8086 and its co-processor.
5. List the operating modes of 8255 A and 8237 A.
6. What freq. transmit clock ( $\overline{TxC}$ ) is required by an 8251 in order for it to transmit data at 4800 baud with a baud rate factor of 16?
7. Mention the number of register banks and their addresses in 8051.
8. What is the jump range?
9. Mention the features of serial port in mode 0.
10. How is A/D converter interfaced with 8051?

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AZHAGAPPAPURAM - 625 401  
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PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the architecture of Intel 8086 with the help of a block diagram. (8)
- (ii) Briefly describe about addressing modes of 8086. (8)

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- (b) Explain in detail about the interrupts and interrupt service routines of 8086. (16)

12. (a) With neat diagram explain the minimum mode of operation of 8086. (16)

Or

- (b) Define loosely coupled system. Explain the schemes used for establishing priority. (16)

13. (a) Draw the block diagram and explain the operations of 8251 serial communication interface. (16)

Or

- (b) Draw the block diagram of programmable interrupt controller and explain its operations. (16)

14. (a) (i) Explain in detail about the Special Function Registers in 8051. (8)
- (ii) Briefly explain about addressing modes of 8051. (8)

Or

- (b) (i) Give PSW of 8051 and describe the use of each bit in PSW. (8)
- (ii) Describe the functions of the following signals in 8051. (8)
- RST, EA, PSEN and ALE.

15. (a) With a neat circuit diagram explain how a 4 × 4 keypad is interfaced with 8051 microcontroller and write 8051 ALP for keypad scanning. (16)

Or

- (b) Draw the schematic for interfacing a stepper motor with 8051 microcontroller and write 8051 ALP for changing speed and direction of motor. (16)

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 27203

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Reg. No.

A U H I P P O . C O M \*



Question Paper Code : 71737

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Fourth/Fifth Semester

Electronics and Communication Engineering

EC 6504 – MICROPROCESSOR AND MICROCONTROLLER

(Common to Biomedical Engineering/Computer Science and Engineering/Medical  
Electronics Engineering/Information Technology)

(Regulations 2013)

Time : Three hours

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Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. The offset address of a data is  $(341B)_H$  and the data segment register value is  $(123A)_H$ . What is the physical address of the data?
2. Define stack register.
3. What is meant by multiprogramming?
4. Write some example for advanced processors.
5. Draw the format of read back command register, of 8254.
6. Write a 16 bit delay program in 8086.
7. Which port used as multifunction port? List the signals.
8. Illustrate the CJNE instruction.
9. List the 8051 interrupts with its priority.
10. What are the types of sensors used for interfacing?

PART B — (5 × 13 = 65 marks)

11. (a) Draw and explain the architecture of 8086 with neat diagram.

Or

- (b) Describe the interrupts of 8086 and its types with service routine.

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12. (a) Explain the system bus structure of 8086. Draw the timing diagram for interrupt acknowledgement cycle.

Or

- (b) Explain the closely looped configuration with neat diagram.

13. (a) Draw and explain the functional diagram of parallel communication interfacing chip.

Or

- (b) Explain the need of DMA controller with its functional diagram.

14. (a) Write the available special function registers in 8051. Explain each register with its format and functions.

Or

- (b) (i) Discuss the types of addressing mode with suitable example in 8051. (8)

- (ii) Write an 8051 assembly language program to multiply the given number 48H and 30H. (5)

15. (a) Write a program for generation of unipolar square waveform of 1 KHz frequency using Timer0 of 8051 in mode0. Consider the system frequency as 12MHz.

Or

- (b) Demonstrate the interfacing of the stepper motor with 8051 and explain its interfacing diagram and develop program to rotate the motor in clock wise direction.

PART C — (1 × 15 = 15 marks)

16. (a) Develop a 8086 based system to display the word HELLO for every 2ms in the common cathode seven segment LED display and check how many times the word displayed for one hour.

Or

- (b) Develop 8051 based system design having 8Kbyte RAM to generate the triangular wave using DAC.



Reg. No.

A U H I P P O . C O M \*



Question Paper Code : 80345

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Fifth Semester

Electronics and Communication Engineering

EC 6504 — MICROPROCESSOR AND MICROCONTROLLER

(Common to Fifth Semester Biomedical Engineering and also common to Fourth Semester Information Technology and Medical Electronics/Computer Science and Engineering)

(Regulations 2013)

Time : Three hours

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Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the flags of 8086 microprocessor.
2. List the segment registers of 8086.
3. Define machine cycle.
4. Define Bus.
5. How DMA is initiated?
6. What is the drawback of memory mapped I/O?
7. Draw the pin diagram of 8051.
8. What is the significance of EA pin?
9. List the modes of Timer in 8051.
10. State how baud rate is calculated for serial data transfer in mode 1.

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PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the internal hardware architecture of 8086 microprocessor with neat diagrams. (12)
- (ii) Write a short note about assembler directives. (4)

Or

- (b) Explain the various addressing modes of 8086 microprocessor with suitable examples. (16)

12. (a) Discuss about the multiprocessor configurations of 8086. (16)

Or

- (b) Explain in detail about the system bus timing of 8086/8088. (16)

13. (a) Explain in detail about DMA controller. (16)

Or

- (b) Explain the procedure of interfacing D/A and A/D converter circuit. (16)

14. (a) Explain in detail about the architecture of 8051 microcontroller with neat diagram. (16)

Or


- (b) Write an ALP using 8051 instructions to receive bytes of data serially and put them in P1. Set the baud rate at 4800, 8-bit data, and 1 stop bit. (16)

15. (a) Describe the different modes of operation of timers/counters in 8051 microcontroller. (16)

Or

- (b) Draw a diagram to interface a stepper motor with 8051 microcontroller also write an 8051 ALP to run the stepper motor in both forward and reverse direction with a delay. (16)

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