ANNAI VAILANKANNI COLLEGE OF ENGINEERING

(A Christian Minority Institution)

Approved by AICTE, New Delhi & Affilliated to Anna University, Chennai

Recognized under section 2(f) of UGC Act 1956

Website: www.avce.edu.in

Dr.R Angeline Prabhavathy

PRINCIPAL

AUTHENTICATION CERTIFICATE

This is to certify that our Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment.

ANNAI VAILANKANNI COLLEGE OF ENGINEERING
POTTALKULAM, AZHAGAPPAPURAM P.O. KANYAKUMARI DISTRICT 629 401

PRINCIPAL

PRINCIPAL
ANNAI VAILANKANNI COLLEGE OF ENGINEERING
POTTALKULAM
AZHAGAPPAPURAM - 629 401
KANYAKUMARI DIST.

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Azhagappapuram Post, Kanyakumari District - 629401.

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1.1.1 The Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment.

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ANNAI VAILANKANNI COLLEGE OF ENGINEERING POTTALKULAM, AZHAGAPPAPURAM P.O. KANYAKUMARI DISTRICT 629 401

PRINCIPAL
ANNAI VAILANKANNI COLLEGE OF ENGINEERING
POTTALKULAM
AZHAGAPPAPURAM - 629 401
KANYAKUMARI DIST.

Date: 02.11.2022

CENTRE FOR ACADEMIC COURSES

ANNA UNIVERSITY: : CHENNAI – 600 025

ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES

November 2022 – April 2023 (SEMESTER I)

UG (FT/PT) Degree Programmes

Sl. No.	Programme	Semester	Commencement of Induction Programme	Commencement of Classes	Last working day	Commencement of Practical Examinations	Commencement of End Semester Examinations
1.	B.E. / B.Tech. (Full Time)	I	14.11.2022	28.11.2022	23.03.2023	25.03.2023	05.04.2023
2.	B.Arch.(Full Time)	I	14.11.2022	28.11.2022	15.03.2023	25.03.2023	05.04.2023
3.	B.E. / B.Tech. (Part Time)	I	-	14.11.2022	01.03.2023	25.03.2023	05.04.2023

RE-OPENING DAY FOR THE NEXT SEMESTER: 15.05.2023 (Monday)

NOTE:

1. The Theory and Practical Examination schedules will be published in due course. (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

02/11/2022

PRINCIPAL
ANNAI VAILANKANNI COLLEGE OF ENGINEERING
POTTALKULAM
AZHAGAPPAPURAM - 629 401
KANYAKUMARI Dist.

DIRECTOR
ACADEMIC COURSES

DAC : 88

1

Date: 02.11.2022

REVISED - I

CENTRE FOR ACADEMIC COURSES

ANNA UNIVERSITY: : CHENNAI – 600 025

ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES

August 2022 – December 2022 (Semester III)

UG (FT/PT) & PG (FT/PT) Degree Programmes

Sl. No.	Programme	Semester	Commencement of Classes	Last working day		Commencement of Practical Examinations		Commencement of End Semester Examinations	
				Existing	Revised	Existing	Revised	Existing	Revised
1.	B.E. / B.Tech. (Full-Time)	III	22.08.2022	08.12.2022	27.12.2022	10.12.2022	18.01.2023	21.12.2022	29.12.2022
2.	B.Arch. (Full-Time)	III	22.08.2022	08.12.2022	-	10.12.2022	18.01.2023	21.12.2022	29.12.2022
3.	B.E. / B.Tech (Part-Time)	III							
4.	M.B.A. (5 Yrs-Integrated)	III							
5.	M.B.A. (Full-Time & Part-Time)	III	01.09.2022	19.12.2022	-	21.12.2022	18.01.2023	02.01.2023	29.12.2022

RE - OPENING DAY FOR THE NEXT SEMESTER: 01.02.2023 (Wednesday)

NOTE:

1. The Theory and Practical Examination schedules will be published in due course (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

PRINCIPAL
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02/11/2022

DIRECTOR
ACADEMIC COURSES

DAC - 58

2

Date: 02.11.2022

REVISED

CENTRE FOR ACADEMIC COURSES

ANNA UNIVERSITY: : CHENNAI – 600 025

ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES

August 2022 – December 2022 (ODD SEMESTER – Except Semester III)

UG Programmes

Sl. No	Programme	Semester	Commencement of Classes	Last working day		Commencement of Practical Examinations		Commencement of End Semester Examinations	
				Existing	Revised	Existing	Revised	Existing	Revised
1.	B.E. / B.Tech.(Full-Time)	V, VII	10.08.2022	19.11.2022	06.12.2022**	21.11.2022	18.01.2023	01.12.2022	08.12.2022
2.	B.E. / B.Tech (Part-Time)	V, VII	10.08.2022	19.11.2022	-	21.11.2022	-	01.12.2022	-
3.	B.Arch. (Full-Time)	V, VII, IX							

RE - OPENING DAY FOR THE NEXT SEMESTER: 30.01.2023 (Monday)

NOTE:

1. The Theory and Practical Examination schedules will be published in due course (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

** In order to ensure minimum no. of working days, the following Saturdays are declared as working days.

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
1.	20.08.2022	Monday
2.	03.09.2022	Friday
3.	17.09.2022	Wednesday
4.	15.10.2022	Tuesday
5.	29.10.2022	Wednesday

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
6.	05.11.2022	Monday
7.	12.11.2022	Tuesday
8.	19.11.2022	Wednesday
9.	26.11.2022**	Thursday
10.	03.12.2022**	Friday

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02/11/2022

DIRECTOR
ACADEMIC COURSES

DAC - 58

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Date: 06.10.2022

CENTRE FOR ACADEMIC COURSES

ANNA UNIVERSITY: : CHENNAI – 600 025

ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES

October 2022 – February 2023 (Odd Semester – Semester I)

PG (FT) Degree Programmes

Sl. No	Programme	Semester	Commencement of Classes	Last working day	Commencement of Practical Examinations	Commencement of End Semester Examinations
1.	M.E. / M. Tech. / M. Arch.(FT)	I	10.10.2022	25.01.2023	27.01.2023	06.02.2023

RE-OPENING DAY FOR THE NEXT SEMESTER: 08.02.2023 (Wednesday)

NOTE:

1. The Theory and Practical Examination schedules will be published in due course. (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

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DIRECTOR I/c
ACADEMIC COURSES

CAC - 88

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Date: 02.11.2022

CENTRE FOR ACADEMIC COURSES

ANNA UNIVERSITY: : CHENNAI – 600 025

ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES

December 2022 – April 2023 (Odd Semester –Semester III)

PG (FT) Degree Programmes

Sl. No	Programme	Semester	Commencement of Classes	Last working day	Commencement of Practical Examinations	Commencement of End Semester Examinations
1.	M.E. / M. Tech. / M. Arch.(FT)	III	12.12.2022	23.03.2023	25.03.2023	05.04.2023

RE-OPENING DAY FOR THE NEXT SEMESTER: 15.05.2023 (Monday)

** In order to ensure minimum no. of working days, the following Saturdays are declared as working days.

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
1.	24.12.2022	Monday
2.	07.01.2023	Tuesday
3.	21.01.2023	Wednesday

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
4.	04.02.2023	Wednesday
5.	18.02.2023	Friday

1. Theory and Practical Examination schedules will be published in due course. (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

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02/11/2022

DIRECTOR
ACADEMIC COURSES

DAC - SB

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Date: 04.05.2023

CENTRE FOR ACADEMIC COURSES

ANNA UNIVERSITY: : CHENNAI – 600 025

ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES

May 2023 – August 2023 (Even Semester)

UG (FT/PT) & PG (FT) Degree Programmes

Sl. No.	Programme	Semester	Commencement of Classes	Last working day	Commencement of Practical Examinations	Commencement of End Semester Examinations
1.	B.E. / B.Tech.(Full-Time)	II	10.05.2023	07.08.2023**	09.08.2023	21.08.2023
2.	B.Arch. (Full-Time)	II				
3.	B.E. / B.Tech (Part-Time)	II				
4.	M.E. / M. Tech. / M. Arch. (FT)	IV				

RE - OPENING DAY FOR THE NEXT SEMESTER: 11.09.2023 (Monday)

NOTE:

1. The Theory and Practical Examination schedules will be published in due course (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

** In order to ensure minimum no. of working days, the following Saturdays are declared as working days.

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
1.	13.05.2023	Friday
2.	20.05.2023	Monday
3.	27.05.2023	Tuesday
4.	03.06.2023	Wednesday
5.	10.06.2023	Thursday
6.	17.06.2023	Friday

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
7.	24.06.2023	Monday
8.	01.07.2023	Tuesday
9.	08.07.2023	Wednesday
10.	15.07.2023	Thursday
11.	22.07.2023	Friday
12.	05.08.2023	Monday

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04/05/2023
DIRECTOR
ACADEMIC COURSES

CAC - 58

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Date: 30.03.2023

REVISED

CENTRE FOR ACADEMIC COURSES

ANNA UNIVERSITY: : CHENNAI - 600 025

ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES

February 2023 – June 2023 (Even Semester – Except Semester II)

UG / PG (FT/PT) Degree Programmes

Sl. No.	Programme	Semester	Commencement of Classes	Last working day		Commencement of Practical Examinations		Commencement of End Semester Examinations	
				Existing	Revised	Existing	Revised*	Existing	Revised*
1.	B.E. / B.Tech.(Full-Time)	IV,VI	06.02.2023	12.05.2023	24.05.2023***	15.05.2023	25.05.2023	26.05.2023	05.06.2023
2.	B.E. / B.Tech.(Full-Time)	VIII	06.02.2023	12.05.2023**	-	15.05.2023	-	26.05.2023	-
3.	B.Arch. (Full-Time)	IV,VI,VIII,X							
4.	B.E. / B.Tech. (Part-Time)	IV,VI							
5.	M.B.A.(Full-Time & Part-Time)	IV							
6.	M.B.A. (5 Yrs-Integrated)	IV,VI,VIII,X							

RE - OPENING DAY FOR THE NEXT SEMESTER: 07.08.2023 (Monday)

* To provide additional classes for Skill Based Courses.

NOTE:

1. The Theory and Practical Examination schedules will be published in due course (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

** In order to ensure minimum no. of working days, the following Saturdays are declared as working days.

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
1.	11.02.2023	Monday
2.	18.02.2023	Tuesday
3.	25.02.2023	Wednesday
4.	04.03.2023	Thursday
5.	11.03.2023	Friday
6.	18.03.2023	Monday

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
7.	25.03.2023	Tuesday
8.	01.04.2023	Wednesday
9.	29.04.2023	Thursday
10.	06.05.2023	Friday
11.	13.05.2023	Monday***
12.	20.05.2023	Tuesday***

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POTTALKULAM
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KANYAKUMARI DIST.

30/3/2023

DIRECTOR
ACADEMIC COURSES

DAC - SB

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Date: 27.08.2022

REVISED

CENTRE FOR ACADEMIC COURSES

ANNA UNIVERSITY: : CHENNAI – 600 025

ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES

June 2022 – October 2022 (Even Semester –Semester II)

PG (FT) Degree Programmes

Sl. No	Programme	Semester	Commencement of Classes	Last working day	Commencement of Practical Examinations	Commencement of End Semester Examinations	
						Existing	Revised
1.	M.E. / M. Tech. / M. Arch.(FT)	II	27.06.2022	30.09.2022**	06.10.2022	17.10.2022	26.10.2022

RE-OPENING DAY FOR THE NEXT SEMESTER: 16.11.2022 (Wednesday)

1. Theory and Practical Examination schedules will be published in due course. (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.

** In order to ensure minimum no. of working days, the following Saturdays are declared as working days.

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
1.	02.07.2022	Thursday
2.	16.07.2022	Tuesday
3.	30.07.2022	Friday
4.	13.08.2022	Monday
5.	27.08.2022	Tuesday

Sl. No.	Working Days (Saturdays)	Time Table of the Week Day to be Followed
6.	03.09.2022	Wednesday
7.	10.09.2022	Thursday
8.	17.09.2022	Friday
9.	24.09.2022	Monday

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27/8/2022

DIRECTOR
ACADEMIC COURSES

DAC - 58

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ANNA UNIVERSITY:: CHENNAI 600 025

Internal Assessment Schedule for Non Autonomous Affiliated Institutions

NOVEMBER 2022 – MARCH 2023 - (SEMESTER – I)

UG (FT) Degree Programmes

Report No	Report Period	Test Period	Report Entry Period
I	28-11-2022 – 24-01-2023	18-01-2023 – 24-01-2023	25-01-2023 – 03-02-2023
II	25-01-2023 – 23-03-2023	16-03-2023 – 23-03-2023	23-03-2023 – 25-03-2023

Saturdays may be included as working days to make good the Shortages, if any.

06.01.2023

CONTROLLER OF EXAMINATIONS

06-01-2023

PRINCIPAL
ANNAI VAILANKANNI COLLEGE OF ENGINEERING
POTTALKULAM
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KANYAKUMARI DIST.

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ANNA UNIVERSITY:: CHENNAI 600 025

Internal Assessment Schedule for Non Autonomous Affiliated Institutions

AUGUST 2022 – DECEMBER 2022 - (SEMESTER - III)

UG (FT&PT) & PG(M.B.A) (5yrs Integrated) Degree Programmes

Report No	Report Period	Test Period	Report Entry Period
I	22-08-2022 – 15-10-2022	10-10-2022 – 15-10-2022	15-10-2022 – 21-10-2022
II	17-10-2022 – 08-12-2022	02-12-2022 – 08-12-2022	08-12-2022 – 10-12-2022

Saturdays may be included as working days to make good the Shortages, if any.

P. Santhivel
19-09-2022
CONTROLLER OF EXAMINATIONS

10
19.9.22

PRINCIPAL
ANNAI VAILANKANNI COLLEGE OF ENGINEERING
KULAM
- 625 401
DIST.

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ANNA UNIVERSITY:: CHENNAI 600 025

Internal Assessment Schedule for Non Autonomous Affiliated Institutions

AUGUST2022 - DECEMBER 2022 - For all UG - Programmes (ODD SEMESTER-EXCEPT III SEMESTER)

Report No	Report Period	Test Period	Report Entry Period
I	10-08-2022 –23-08-2022	----	29-09-2022 – 06-10-2022
II	24-08-2022 – 21-09-2022	16-09-2022 – 21-09-2022	29-09-2022 – 06-10-2022
III	22-09-2022 – 21-10-2022	17-10-2022 – 21-10-2022	21-10-2022 –29-10-2022
IV	22-10-2022 – 19-11-2022	14-11-2022 – 19-11-2022	19-11-2022 – 21-11-2022

Saturdays may be included as working days to make good the Shortages, if any.

19.09.2022
CONTROLLER OF EXAMINATIONS

19.09.22

PRINCIPAL
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ANNA UNIVERSITY:: CHENNAI 600 025

Internal Assessment Schedule for Non Autonomous Affiliated Institutions

OCTOBER 2022 – JANUARY 2023 - (SEMESTER – I)

PG (FT & PT) Degree Programmes - M.E.A&M.E.BA(INTEGRATED)

Report No	Report Period	Test Period	Report Entry Period
I	10-10-2022 – 02-12-2022	28-11-2022 – 02-12-2022	19-12-2022 – 23-12-2022
II	03-12-2022 – 25-01-2023	20-01-2023 – 25-01-2023	25-01-2023 – 27-01-2023

Saturdays may be included as working days to make good the Shortages, if any.

PRINCIPAL
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19-12-2022

CONTROLLER OF EXAMINATIONS

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ANNA UNIVERSITY:: CHENNAI 600 025

Internal Assessment Schedule for Non Autonomous Affiliated Institutions

DECEMBER 2022 – MARCH 2023 - (SEMESTER – III)

PG (FT) Degree Programmes - M.E. / M.Tech. / M.Arch.

Report No	Report Period	Test Period	Report Entry Period
I	12-12-2022 – 01-02-2023	27-01-2023 – 01-02-2023	01-02-2023 – 07-02-2023
II	02-02-2023 – 23-03-2023	17-03-2023 – 23-03-2023	23-03-2023 – 25-03-2023

Saturdays may be included as working days to make good the Shortages, if any.

PRINCIPAL
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29.12.2022

CONTROLLER OF EXAMINATIONS

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ANNA UNIVERSITY:: CHENNAI 600 025

Internal Assessment Schedule for Non Autonomous Affiliated Institutions

April 2022 – July 2022 - (SEMESTER - II)

B.E./B.TECH.(FT/PT) Degree Programmes & M.B.A. (FT/PT/5 Yrs - Integrated) Degree Programmes

Report No	Report Period	Test Period
I	04-04-2022 -- 21-05-2022	16-05-2022 -- 21-05-2022
II	23-05-2022 -- 04-07-2022	28-06-2022 -- 04-07-2022

April 2022 – July 2022 - (SEMESTER - II)

B.ARCH.(FT) Degree Programme

Report No	Report Period	Test Period
I	04-04-2022 -- 06-05-2022	29-04-2022 -- 06-05-2022
II	07-05-2022 -- 04-06-2022	30-05-2022 -- 04-06-2022
III	06-06-2022 -- 04-07-2022	28-06-2022 -- 04-07-2022

Saturdays may be included as working days to make good the Shortages, if any.

PRINCIPAL
ANNAI THANGAMMAL MEGALA COLLEGE OF ENGINEERING
PATTALIKULAM
ACHARAPAKKAM - 603 301
KANYAKUMARI DIST.

09/05/2022

09.05.2022

09.05.2022
CONTROLLER OF EXAMINATIONS (I/c)

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ANNA UNIVERSITY:: CHENNAI 600 025

OFFICE OF THE CONTROLLER OF EXAMINATION

February 2023 – May 2023 - (SEMESTER - IV) – R-2021

FOR ALL UG /PG(MBA) PROGRAMMES

Report No	Report Period	Test Period	Report Entry Period
I	06-03-2023 – 21-03-2023	15-03-2023 – 21-03-2023	21-03-2023 – 28-03-2023
II	23-03-2023 – 12-05-2023	08-05-2023 – 12-05-2023	12-05-2023 – 15-05-2023

Saturdays may be included as working days to make good the shortages, if any.

13.03.2023

CONTROLLER OF EXAMINATIONS

13/03/2023

13.03.23

PRINCIPAL

ASHOK VALANKANI COLLEGE OF ENGINEERING

AZHAR

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ANNA UNIVERSITY :: CHENNAI 600 025

Internal Assessment Schedule for Non Autonomous Affiliated Institutions

MARCH - JUNE 2022 - For all UG - Programmes (Even Semester – Except Semester II)

Report No	Report Period	Test Period	Report Entry Period
I	16-03-2022 – 01-04-2022	----	21-04-2022 – 25-04-2022
II	04-04-2022 – 29-04-2022	25-04-2022 – 29-04-2022	29-04-2022 – 04-05-2022
III	30-04-2022 – 24-05-2022	19-05-2022 – 24-05-2022	24-05-2022 –28-05-2022
IV	25-05-2022 – 16-06-2022	11-06-2022 – 16-06-2022	16-06-2022 – 17-06-2022

Saturdays may be included as working days to make good the Shortages, if any.

20.04.2022

CONTROLLER OF EXAMINATIONS

PRINCIPAL
ARNAV VALLIAMMAI COLLEGE OF ENGINEERING
POTHALKULAM
AZHAGAPPAPURAM - 623 401
RAMANATHAPURAM DIST.

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ANNAI VAILANKANNI COLLEGE OF ENGINEERING

MASTER ACADEMIC CALENDAR

ACADEMIC CALENDAR 2022 -2023 (ODD) -S3,S5 & S7

WORKING DAYS =85 (S5,S7) / 93 (S3)

		AUGUST			SEPTEMBER			OCTOBER			NOVEMBER			DECEMBER	
DAY	DATE		WD	DATE		WD	DATE		WD	DATE		WD	DATE		WD
SUN		Holiday			Holiday		2	GANDHI JEYANTHI			Holiday			Holiday	
MON	1						3	Holiday							
TUE	2						4	Holiday		1	KANYAKUMARI DAY				
WED	3						5		1	2	Coaching	1			
THU	4			1		1	6		2	3	Coaching	2	1		81
FRI	5			2		2	7		3	4	Coaching	3	2		82
SAT	6			3		3	8			5	Coaching	4	3		83
SUN	7	Holiday		4	Holiday		9	Holiday		6	Holiday		4	Holiday	
MON	8			5	CT 2	4	10		4	7	Naan Mudhalvan	5	5		84
TUE	9			6	CT 2 - RESULT ANALYSIS	5	11		5	8	Naan Mudhalvan	6	6	Last	85
WED	10	Commencement of classes (S5,S7)	1	7		6	12		6	9	Naan Mudhalvan	7	7		
THURS	12	CT 1	2	9	Completion of Unit 2	7	14	Completion of Unit 4	7	11	Naan Mudhalvan	8	9		
FRI	11		3	8		8	13	Industrial visit for III	8	10	Naan Mudhalvan	9	8	Commencem	
SAT	13			10			15			12		10	10		
SUN	14	Holiday		11			16			13	Deepavali		11	Holiday	
MON	15	NDEPENDENCE DAY		12	IAT 1	9	17	IAT 2	9	14	Model Exam	11	12		
TUE	16		4	13		10	18		10	15	Model Exam	12	13		
WED	17		5	14		11	19		11	16	Model Exam	13	14		
THU	18		6	15		12	20		12	17	Model Exam	14	15	Innovation day	
FRI	19	Holiday		16	IAT 1 - RESULT ANALYSIS	13	21	T 2 - RESULT ANALY	13	18	Model Exam	15	16		
SAT	20		7	17			22			19	Model Exam	16	17		
SUN	21	Holiday		18	Ganesh chaturthi		23	Holiday		20	Holiday		18	Holiday	
MON	22	mencement of classes	8	19	CCM	14	24	Diwali		21		17	19		
TUE	23		9	20		15	25	Holiday		22		18	20		
WED	24	tion of Unit I/Mech-w	10	21		16	26	CCM	14	23		19	21		
THU	25		11	22		17	27		15	24	CAAD EVENT	20	22		
FRI	26	Webinar	12	23		18	28		16	25		21	23		
SAT	27			24			29			26		22	24		
SUN	28	Holiday		25	Holiday		30			27	Holiday		25	Holiday	
MON	29		13	26		19	31	CT 4	17	28			26		
TUE	30	Workshop	14	27		20				29		24	27	1 woking day (S3)	
WED	31		15	28		21				30		25	28		
THU				29		22							29	Commencem	
FRI				30	Completion of Unit 3	23							30		
SAT						24									
		WD=15 (S5,S7)			WD=24 (S3,S5,S7)			WD=17 (S3,S5,S7)			WD=25 (S3,S5,S7)			WD=5 (S5,S7)	
		WD=8 (S3)												WD= 19 (S3)	

WD - Working Days IAT - Internal Accessament Test CCM-Class Committee Meeting CT-Cycle test

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KANYAKUMARI DIST.

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC CALENDAR 2022 -2023 (EVEN) -S4,S6,S8

TOTAL WORKING DAYS =81

		JANUARY			FEBRUARY			MARCH			APRIL			MAY	
DAY	DATE		WD	DATE		WD	DATE		WD	DATE		WD	DATE		WD
SUN	1	Holiday			Holiday			Holiday			Holiday			Holiday	
MON	2												1	May Day	
TUE	3												2		62
WED	4			1			1	Workshop	20				3		63
THU	5			2			2		21				4		64
FRI	6			3			3		22				5		65
SAT	7			4			4	Holiday		1		44	6		66
SUN	8	Holiday		5	Holiday		5	Holiday		2	Holiday		7	Holiday	
MON	9			6	Commencement of II,III & IV Year Classes	1	6	CT	23	3		45	8		67
TUE	10			7		2	7	CT	24	4	Mahaveer Jayanthi		9		68
WED	11			8		3	8		25	5		46	10		69
THU	12			9		4	9		26	6		47	11		70
FRI	13			10	Guest Lecture	5	10		27	7	Good Friday		12		71
SAT	14	Holiday		11		6	11		28	8	Holiday		13		72
SUN	15	Holiday		12	Holiday		12	Holiday		9	Holiday		14	Holiday	
MON	16			13		7	13		29	10		48	15	MODEL	73
TUE	17			14		8	14		30	11	Guest Lecture	49	16	MODEL	74
WED	18			15		9	15	IAT-I	31	12		50	17	MODEL	75
THU	19			16		10	16	IAT-I	32	13		51	18	MODEL	76
FRI	20			17		11	17			14	Tamil New Year Day		19	MODEL	77
SAT	21			18	Holiday		18	IAT-I	33	15	Holiday		20		78
SUN	22	Holiday		19	Holiday		19	Holiday		16	Holiday		21	Holiday	
MON	23			20		12	20	IAT-I	34	17	IAT-II	52	22	MODEL	79
TUE	24			21		13	21	CCM	35	18	IAT-II	53	23		80
WED	25			22		14	22	Telugu New Year Day		19	IAT-II	54	24	Last working Day	81
THU	26			23		15	23		36	20	CCM	55	25		
FRI	27			24		16	24		37	21		56	26		
SAT	28			25		17	25		38	22	Ramzan		27		
SUN	29	Holiday		26	Holiday		26	Holiday		23	Holiday		28	Holiday	
MON	30			27	CT	18	27		39	24			29		
TUE	31			28	CT	19	28		40	25		57	30		
WED							29		41	26		58	31		
THU							30		42	27		59			
FRI							31		43	28		60			
SAT										29		61			
					WD=19			WD=24		30	WD=18			WD=20	

WD - Working Days IAT - Internal Acessesment Test CCM-Class Committee Meeting CT-Cycle test

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ANNAI VAILANKANNI COLLEGE OF ENGINEERING

Azhagappapuram.P.O, K.K.District ,Tamil Nadu - 629 401

Faculty Workload w.e.f A.Y 2022-23(Even Semester)

Department of Electronics and communication Engineering W.e.f.-06-Feb-2023

Sl. No	Name of Faculty and Designation	SUBJECT		T/P	Semester/ Dept/Asst
		CODE	NAME		
1	Dr. Abilash	EC 8811	Project Work	T	08/ECE
2	Dr. Shaheer Abubacker	GE 8076	Professional Ethics In Engineering	T	08/ECE
3	Dr. Narendra Kumar.A	EC 8094	Satellite Communication	T	08/ECE
4	Dr. Vinoth	EC3452	Electromagnetic Fields	T	04/ECE
	Professor	EC8611	Technical Seminar (TS)	P	06/ECE
5	Mrs. Bagavathy	EC3401	Networks and Security & Lab	T/P	04/ECE
		EC8095	VLSI Design	T	06/ECE
	Assistant Professor	EC8661	VLSI Design Laboratory	P	06/ECE
6	Mrs.P.Renuka	EC8691	Microprocessors and Microcontrollers	T	06/ECE
		EC8681	Microprocessors and Microcontrollers Lab (MPMC LAB)	P	06/ECE
	Assistant Professor	EC8002	Multimedia Compression and Communication	T	06/ECE
7	Mr.R.Robert	EC3492	Digital Signal Processing & Lab	T/P	04/ECE
	Assistant Professor	MG8591	Principles of Management	T	06/ECE
8	Ms.T.Sreeja	EC8652	Wireless Communication	T	06/ECE
		EC3491	Communication Systems	T	04/ECE
	Assistant Professor	EC3461	Communication Systems Laboratory	P	04/ECE
9	Mrs.E.Rajeswari	EC8651	Transmission Lines and RF Systems	T	06/ECE
	Assistant Professor	EC3451	Linear Integrated Circuits	T	04/ECE
		EC3462	Linear Integrated Circuits Laboratory	P	04/ECE

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ANNAI VAILANKANNI COLLEGE OF ENGINEERING

Azhagappapuram,P.O, K.K.District ,Tamil Nadu - 629 401

Department of Electronics and Communication Engineering W.e.f.-06-FEB 2023

TIME TABLE - 2022 to 2023 (EVEN)

Class : II YEAR

Sem. : IV

HRS	1	2	BREAK	3	4	LUNCH BREAK	5	6	7
DAY	9.00 - 9.50	9.50 - 10.40		10.50-11.40	11.40-12.30		1.00-1.50	2.00-2.50	2.50-3.40
DAY 1	EMF	LIC		CS	NS		ESS	DSP	LIC
DAY 2	DSP	NS		LIC	EMF		LIC	DSP	ESS
DAY 3	EMF	CS		DSP	ESS		EMF	NS	DSP
DAY 4	NS	ESS		CS	EMF		LIC LAB	LIC LAB	
DAY 5	ESS	CS		DSP	NS		CS LAB	CS LAB	

Sl.No	SUBJECT CODE	NAME OF THE SUBJECT	L/P	FACULTY ALLOTED
1	EC3452	Electromagnetic Fields	L	Dr. Vinoth
2	EC3401	Networks and Security & Lab	L	Mrs. Bagavathy
3	EC3451	Linear Integrated Circuits	L	Mrs.P.Rajeswari
4	EC3492	Digital Signal Processing & Lab	L	Mr.R.Robert
5	EC3491	Communication Systems	L	Ms. Sreeja
6	GE3451	Environmental Sciences and Sustainability	L	Dr. Sona Selva Malar
		LABORATORY CLASSES		
7	EC3461	Communication Systems Laboratory	P	Ms. Sreeja
8	EC3462	Linear Integrated Circuits Laboratory	P	Mrs.P.Rajeswari

Class : III YEAR

Sem. : 06

HRS	1	2	BREAK	3	4	LUNCH BREAK	5	6	7
DAY	9.00 - 9.50	9.50 - 10.40		10.50-11.40	11.40-12.30		1.00-1.50	2.00-2.50	2.50-3.40
DAY 1	MPMC	POM		MCC	VLSI		TRS	WC	MCC
DAY 2	TRS	WC		VLSI	MCC		MPMC	PC	POM
DAY 3	POM	WC		TRS	MPMC		MCC	WC	VLSI
DAY 4	VLSI	MPMC		TS	WC		VLSI LAB	VLSI LAB	
DAY 5	TRS	VLSI		TRS	POM		MPMC LAB	MPMC LAB	

Sl.No	SUBJECT CODE	NAME OF THE SUBJECT	L/P	FACULTY ALLOTED
1	EC8095	VLSI Design	L	Mrs. Bagavathy
2	EC8652	Wireless Communication	L	Ms. Sreeja
3	MG8591	Principles of Management	L	Mr.R.Robert
4	EC8651	Transmission Lines and RF Systems	L	Mrs.P.Rajeswari
5	EC8002	Multimedia Compression and Communication	L	Mrs.P.Renuka
6	EC8691	Microprocessors and Microcontrollers	L	Mrs.P.Renuka
		LABORATORY CLASSES		
7	EC8681	Microprocessors and Microcontrollers Lab (MPMC LAB)	P	Mrs.P.Renuka
8	EC8661	VLSI Design Laboratory	P	Mrs. Bagavathy
9	EC8611	Technical Seminar (TS)	P	Dr. Vinoth
10	HS8581	Professional Communication	P	Dr. Renolin Jayanth

Class : IV YEAR

Sem. : 08

HRS	1	2	BREAK	3	4	LUNCH BREAK	5	6	7
DAY	9.00 - 9.50	9.50 - 10.40		10.50-11.40	11.40-12.30		1.00-1.50	2.00-2.50	2.50-3.40
1	PEE	PROJECT		SC	PROJECT		PROJECT	PROJECT	
2	PEE	SC		PROJECT			PROJECT	PROJECT	
3	SC	PROJECT		PEE	PROJECT		PROJECT	PROJECT	
4	PROJECT			PEE	SC		PROJECT	PROJECT	
5	PEE	SC		PROJECT			PROJECT	PROJECT	

Sl.No	SUBJECT CODE	NAME OF THE SUBJECT	L/P	FACULTY ALLOTED
1	GE 8076	Professional Ethics In Engineering	L	Dr. Shaheer Abubacker
2	EC 8094	Satellite Communication	L	Dr. Narendra Kumar.A
		LABORATORY CLASS		
3	EC 8811	Project Work	P	Dr.K.S.Ahilash

HOD

Principal

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

(Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai)

AVK Nagar, Pothaiyadi Salai, Pottalkulam

Azhagappapuram Post, Kanyakumari District - 629 401

COURSE FILE

NAME OF THE FACULTY	:	P.RENUKA
DESIGNATION	:	ASSISTANT PROFESSOR
DEPARTMENT	:	ECE
SUBJECT CODE	:	EC-8691
SUBJECT NAME	:	MICROPROCESSORS AND MICROCONTROLLERS
COURSE	:	BE
YEAR	:	III
SEMESTER	:	06
ACADEMIC YEAR	:	2022-2023(EVEN)
NO OF STUDENTS	:	17

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Contents of Course File

1. Course Objective
2. Academic Schedule
3. Time Table
4. Syllabus
5. Lecture Plan
6. Minimum 5 Sets Of University Question Papers
7. Students Name List
8. Unit Wise 2 Mark Questions with Answers
9. Unit Wise Part – B Question Bank (All Possible Part-B Questions)
10. Assignment
11. Class Test
12. Students Seminar /Video class Details
13. All Class Test Questions
14. Internal Test Questions with Answer Key
15. Sample Test Papers
16. Log Book
17. Class Committee Report
18. Students Feedback
19. CO PO Mapping

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Content of the Course File

1. **Course Objective:**

(Please write few sentences about the objective of offering this subject)

- To understand the Architecture of 8086 microprocessor.
- To learn the design aspects of I/O and Memory Interfacing circuits.
- To interface microprocessors with supporting chips,
- To study the Architecture of 8051 microcontroller
- To design a microcontroller based system

2. **Target Result:**
3. First class with distinction : 30%
4. First Class 50%
5. Pass

6. **Course Plan:**
   a. Teaching the students in the class
   b. Explain the lesion using examples
   c. Explain the practical applications
   d. Presentations through OHP, LCD Projector
   e. Guest lectures on industrial related topics
   f. Teaching with using experiments in lab
7. **Method of Evaluation:**
   a. Class Tests
   b. Internal Examinations (Objective type)
   c. Unit wise Assignments (from previous question papers)
   d. Final examination (Theory / Descriptive type)
8. **Guidelines to students:**
   a. They should attend all the classes to understand and learn basics of this course.
   b. They should go through different text books, internet browsing, journals, news papers to acquire the best and latest knowledge of the subject.
   c. They should learn the things in the practical approach besides theory.
   d. They should gain knowledge by using internet, news papers and journals.

ANJAI VAIYANKANNI COLLEGE OF ... POTTALKUDAIYUR AZHAGAPPAPURAM P.O KANYAKUMARI DISTRICT

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AZHAGAPPAPURAM ...
KANYAKUMARI DIST.

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

AVK Nagar, Pothayadi Salai
Azhagappapuram Post – 629 401, K.K.Dist, Tamil Nadu.

NAME OF THE DEPARTMENT : ELECTRONICS AND COMMUNICATION

YEAR / SEM/SEC : III / 06

SUBJECT CODE : EC 8691

NAME OF THE SUBJECT : Microprocessors and Microcontrollers

NAME OF THE STAFF : Mrs. P. RENUKA

NAME OF THE EXAMINATION	IAT1	IAT2	IAT3
Total Number of students	10	10	10
Number of students absent	02	03	03
Number of students passed	06	06	05
Number of students failed	02	01	02
Percentage of pass	60%	60%	50%

RESULT ANALYSIS

TEST	Below 50	B Grade	B+ Grade	A Grade	A+ Grade	O Grade
IAT1	02	02	02	02		
IAT2	01	01	03	02		
IAT3						
Model	02	01	01	01	02	

STAFF IN CHARGE

HOD

ANNAI VAILANKANNI COLLEGE OF ENGINEERING POTTALKUDAL AZHAGAPPAPURAM P.O. KANYAKUMARI DISTRICT 629 401

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ANNAI VAILANKANNI COLLEGE OF ENGINERING

SF-PNRT-39

Avk Nagar, Pothayadi Salai, Pottalkulam, Azhagappapuram Post - 629401

Student's Seminar / Video Lecture Report

2022/2023 (Odd/Even)

Name of the Faculty : Mrs. P. Renuka

Branch: ECE

Subject Code / Name : EC8691 – Microprocessors and Microcontrollers

Year / Semester:

Sl.No	Date	Period	Student's Name	Topic	Reference (For Video Lecture)	Staff Sign	HOD
1	7/2/23	5	AshanAkthar	Microprocessor			
2	8/2/23	4	Ganga	8086 features			
3	9/2/23	7	Ganga Devi	Flag registers			
4	13/2/23	3	Makenth	Memory			
5	14/2/23	5	Siva Raj	Segment Registers			
6	15/2/23	4	Sri Vindha	Instructions			
7	16/2/23	7	Sneka	Linker			
	20/2/23	1	Ganga	Assembler			
9	21/2/23	5	Ganga Devi	programming			
10	23/2/23	2	Ashish	Stack			
11	25/2/23	1	Santhiya	Loop instructions			
12	27/2/23	1	Thamira	Strings			
13	28/2/23	5	Ganga	Byte Manipulation			
14							
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31							

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ANNAI VAILANKANNI COLLEGE OF ENGINEERING

Pottalkulam, Azhagappapuram P.O., Kanyakumari District – 629 401

ASSIGNMENT DETAILS

Semester & Branch : III - ECE

Subject Code & Name : EC8691 – Microprocessors and Microcontrollers

Name of the Staff : Mrs. P. Renuka

Department : ECE

Assignment No	Topic	Date of Issue	Date of Submission	Date of Correction
01	Assembler Directives of 8086.	16/2/23	20/2/23	21/2/23
02	Maximum	28/2/23	2/3/23	6/3/23
03	Keyboard Interfacing	15/3/23	20/3/23	21/3/23
04	I/O ports, pins and Circuits	5/4/23	8/4/23	10/4/23
05	Stepper Motor interfacing	24/4/23	26/4/23	28/4/23

Signature of the Staff

HOD

Principal

Attachments:

1. Assignment Copies for each

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AZHAGAPPAPURAM - 629 401
KANYAKUMARI DIST.

ANNAI VAILA' ANNI COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC CALENDAR 2022 -2023 (EVEN) -S4,S6,S8

TOTAL WORKING DAYS =81

DAY	DATE	JANUARY	WD	DATE	FEBRUARY	WD	DATE	MARCH	WD	DATE	APRIL	WD	DATE	MAY	WD
SUN	1	Holiday			Holiday			Holiday			Holiday			Holiday	
MON	2												1	May Day	
TUE	3												2		62
WED	4			1			1	Workshop	20				3		63
THU	5			2			2		21				4		64
FRI	6			3			3		22				5		65
SAT	7			4			4	Holiday		1		44	6		66
SUN	8	Holiday		5	Holiday		5	Holiday		2	Holiday		7	Holiday	
MON	9			6	Commencement of II,III & IV Year Classes	1	6	CT	23	3		45	8		67
TUE	10			7		2	7	CT	24	4	Mahaveer Jayanthi		9		68
WED	11			8		3	8		25	5		46	10		69
THU	12			9		4	9		26	6		47	11		70
FRI	13			10	Guest Lecture	5	10		27	7	Good Friday		12		71
SAT	14	Holiday		11		6	11		28	8	Holiday		13		72
SUN	15	Holiday		12	Holiday		12	Holiday		9	Holiday		14	Holiday	
MON	16			13		7	13		29	10		48	15	MODEL	73
TUE	17			14		8	14		30	11	Guest Lecture	49	16	MODEL	74
WED	18			15		9	15	IAT-I	31	12		50	17	MODEL	75
THU	19			16		10	16	IAT-I	32	13		51	18	MODEL	76
FRI	20			17		11	17			14	Tamil New Year Day		19	MODEL	77
SAT	21			18	Holiday		18	IAT-I	33	15	Holiday		20		78
SUN	22	Holiday		19	Holiday		19	Holiday		16	Holiday		21	Holiday	
MON	23			20		12	20	IAT-I	34	17	IAT-II	52	22	MODEL	79
TUE	24			21		13	21	CCM	35	18	IAT-II	53	23		80
WED	25			22		14	22	Telugu New Year Day		19	IAT-II	54	24	Last working Day	81
THU	26			23		15	23		36	20	CCM	55	25		
FRI	27			24		16	24		37	21		56	26		
SAT	28			25		17	25		38	22	Ramzan		27		
SUN	29	Holiday		26	Holiday		26	Holiday		23	Holiday		28	Holiday	
MON	30			27	CT	18	27		39	24			29		
TUE	31			28	CT	19	28		40	25		57	30		
WED							29		41	26		58	31		
THU							30		42	27		59			
FRI							31		43	28		60			
SAT										29		61			
					WD=19			WD=24		30	WD=18			WD=20	

WD - Working Days IAT - Internal Acessesment Test CCM-Class Committee Meeting CT-Cycle test

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POTTAVELLUR
AZHAGAPPAPURAM - 614 701
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ANNAI VAILANKANNI COLLEGE OF ENGINEERING

Azhagappapuram.P.O, K.K.District ,Tamil Nadu - 629 401

Department of Electronics and Communication Engineering W.e.f.-18-FEB 2023

UG TIME TABLE - 2022 to 2023 (EVEN)

Class : III YEAR Sem. : 06

HRS	1	2	BREAK	3	4	LUNCH BREAK	5	6	7
DAY	9.00 - 9.50	9.50 - 10.40		10.50-11.40	11.40-12.30		1.00-1.50	2.00-2.50	2.50-3.40
DAY 1	MPMC	POM		MCC	VLSI		TRS	WC	MCC
DAY 2	TRS	WC		VLSI	MCC		MPMC	PC	POM
DAY 3	POM	WC		TRS	MPMC		MCC	WC	VLSI
DAY 4	VLSI	MPMC		TS	WC		VLSI LAB	VLSI LAB	
DAY 5	TRS	VLSI		TRS	POM		MPMC LAB	MPMC LAB	

Class Advisor :Mrs.E.Rajeswari

TOTAL NUMBER OF STUDENTS: 14

SLNo	SUBJECT CODE	NAME OF THE SUBJECT	L/P	FACULTY ALLOTED
1	EC8095	VLSI Design	L	Mrs.E.Rajeswari
2	EC8652	Wireless Communication	L	Dr. Supriya
3	MG8591	Principles of Management	L	Dr. Vinoth
4	EC8651	Transmission Lines and RF Systems	L	Dr. Leonard Gibson
5	EC8002	Multimedia Compression and Communication	L	Mr. R.Robert
6	EC8691	Microprocessors and Microcontrollers	L	Mrs.P.Renuka
		LABORATORY CLASSES		
7	EC8681	Microprocessors and Microcontrollers Lab (MPMC LAB)	P	Mrs.P.Renuka
8	EC8661	VLSI Design Laboratory	P	Mrs.E.Rajeswari
9	EC8611	Technical Seminar (TS)	P	Dr. Shaheer Ahubacker
10	HS8581	Professional Communication	P	Dr. Narendra Kumar.A

HOD
Date:

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ANNAI VAILANKANNI COLLEGE OF ENGINEERING
POTTAKOTTAI
AZHAGAPPAPURAM - 629 401
KANYAKUMARI DIST.

Principal
Date:

EC8691 MICROPROCESSORS AND MICROCONTROLLERS L T P C
3 0 0

3OBJECTIVES:

- To understand the Architecture of 8086 microprocessor.
- To learn the design aspects of I/O and Memory Interfacing circuits.
- To interface microprocessors with supporting chips.
- To study the Architecture of 8051 microcontroller.
- To design a microcontroller based system

UNIT I THE 8086 MICROPROCESSOR 9

Introduction to 8086 – Microprocessor architecture – Addressing modes - Instruction set and assembler directives – Assembly language programming – Modular Programming - Linking and Relocation - Stacks - Procedures – Macros – Interrupts and interrupt service routines – Byte and String Manipulation.

UNIT II 8086 SYSTEM BUS STRUCTURE 9

8086 signals – Basic configurations – System bus timing –System design using 8086 – I/O programming – Introduction to Multiprogramming – System Bus Structure – Multiprocessor configurations – Coprocessor, Closely coupled and loosely Coupled configurations – Introduction to advanced processors.

UNIT III I/O INTERFACING 9

Memory Interfacing and I/O interfacing - Parallel communication interface – Serial communication interface – D/A and A/D Interface - Timer – Keyboard /display controller – Interrupt controller – DMA controller – Programming and applications Case studies: Traffic Light control, LED display , LCD display, Keyboard display interface and Alarm Controller.

UNIT IV MICROCONTROLLER 9

Architecture of 8051 – Special Function Registers(SFRs) - I/O Pins Ports and Circuits - Instruction set - Addressing modes - Assembly language programming.

UNIT V INTERFACING MICROCONTROLLER 9

Programming 8051 Timers - Serial Port Programming - Interrupts Programming – LCD & Keyboard Interfacing - ADC, DAC & Sensor Interfacing - External Memory Interface- Stepper Motor and Waveform generation - Comparison of Microprocessor, Microcontroller, PIC and ARM processors

TOTAL: 45 PERIODS

OUTCOMES:

At the end of the course, the students should be able to:

- Understand and execute programs based on 8086 microprocessor.
- Design Memory Interfacing circuits.
- Design and interface I/O circuits.
- Design and implement 8051 microcontroller based systems.

TEXT BOOKS:

1. Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer Systems: The 8086 / 8088 Family - Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007. (UNIT I-III)

2. Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson education, 2011. (UNIT IV-V)

REFERENCES:

1. Doughlas V.Hall, "Microprocessors and Interfacing, Programming and Hardware",TMH,2012

2. A.K.Ray,K.M.Bhurchandi, "Advanced Microprocessors and Peripherals" 3 rd edition, Tata McGrawHill, 2012

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AVK Nagar, Pottalkulam, Azhagappapuram Post, K.K.Dist – 629 401

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE PLAN

File No: AVCE/sTLP/04/2022-23/EVEN

PROGRAMME NAME & CODE	:	B.E. (ECE), 106
SEMESTER	:	6
COURSE NAME	:	MICROPROCESSORS AND MICROCONTROLLERS
COURSE CODE	:	EC8691
COURSE COMPONENT	:	PROFESSIONAL CORE
NAME OF THE COURSE INCHARGE	:	P.RENUKA

I. VISION OF THE INSTITUTION

Community Enhancement through Excellence in Engineering Education.

II. MISSION OF THE INSTITUTION

To Enhance Holistic Development among Engineering Students there-by improving their Personal, Professional and Social Competencies.

III. VISION OF THE DEPARTMENT

To strive to produce knowledgeable and meritorious engineers.

IV. MISSION OF THE DEPARTMENT

To provide training and lectures from eminent professionals and help the students to be well equipped technically.

V. PROGRAMME EDUCATIONAL OBJECTIVES (PEO):

PEO 1: To introduce techniques of magnetic-circuit analysis and introduce magnetic materials
PEO 2: To familiarize the constructional details, the principle of operation
PEO 3:. Prediction of performance
PEO 4: The methods of testing the transformers and three phase transformer connections.
PEO 5: To study the working principles of electrical machines using the concepts of electromechanical energy conversion principles
PEO 6: Derive expressions for generated voltage and torque developed in all Electrical Machines.
PEO 7: To study the working principles of DC machines as Generator types
PEO 8: determination of their no- load/load characteristics
PEO9: starting and methods of speed control of motors
PE10: To estimate the various losses taking place in D.C. Motor and to study the different testing methods to arrive at their performance

VI. PROGRAMME OUTCOMES (PO):

PO1: . Ability to model and analyze electrical apparatus and their application to power system
PO2: Ability to understand and apply basic science, circuit theory, Electro-magnetic field theory control theory and apply them to electrical engineering problems.
PO3: Ability to model and analyze electrical apparatus and their application to power system.
PO4: Ability to understand and analyze power system operation, stability, control and protection.
PO5: Ability to handle the engineering aspects of electrical energy generation and utilization.
PO6: Ability to understand and analyse, linear and digital electronic circuits.
PO7: Ability to review, prepare and present technological developments

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PO8:	Ability to form a group and develop or solve engineering hardware and problems.
PO9:	To understand and apply computing platform and software for engineering problems.
PO10:	To understand ethical issues, environmental impact and acquire management skills.

VII. COURSE PLANNING

A. PREAMBLE:

This is an important basic course while enter into the electrical department. This is one of the core paper of electrical sectors. In this course discussed about the fundamental of magnetic circuits and learn basic laws govern in the magnetic circuit. In this students learn about transformer operation and testing of transformers and electromagnetic conversion basic also easily understand by students and learn about motors and dc generator and type and excitation etc.So the students will get knowledge about machine and working conditions.

B.COURSE OBJECTIVES:

- To understand the Architecture of 8086 microprocessor.
- To learn the design aspects of I/O and Memory Interfacing circuits.
- To interface microprocessors with supporting chips.
- To study the Architecture of 8051 microcontroller.

C. TEXT BOOKS / REFERENCE BOOKS / WEB RESOURCES:

i) TEXT BOOKS:

1. **T1** Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer Systems: The 8086 / 8088 Family - Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007. (UNIT I- III)
2. **T2** Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson education, 2011. (UNITI V)

ii) REFERENCE BOOKS:

R1 Doughlas V.Hall, "Microprocessors and Interfacing, Programming and Hardware",TMH,2012

R2. A.K.Ray,K.M.Bhurchandi, "Advanced Microprocessors and Peripherals" 3rd edition, TataMcGrawHill, 2012

iii) WEB RESOURCES:

W1. http://nptel.ac.in

D. UNITWISE COURSE OUTCOMES, SYLLABUS & ASSESSMENT

UNIT I

Expected Course Outcomes:

After successful completion of this unit, the students will be able to:

CO 1.1 Understand and execute programs based on 8086 microprocessor

Syllabus THE 8086 MICROPROCESSOR

Introduction to 8086 – Microprocessor architecture – Addressing modes - Instruction set and assembler directives – Assembly language programming – Modular Programming - Linking and Relocation - Stacks - Procedures – Macros – Interrupts and interrupt service routines – Byte and String Manipulation.

UNIT II

Expected course outcomes:

After successful completion of this unit, the students will be able to:

CO 2.1 Design Memory Interfacing circuits

Syllabus: 8086 SYSTEM BUS STRUCTURE

8086 signals – Basic configurations – System bus timing –System design using 8086 – I/O programming – Introduction to Multiprogramming – System Bus Structure – Multiprocessor configurations – Coprocessor, Closely coupled and loosely Coupled configurations – Introductionto advanced processors

UNIT -III

Expected course outcomes:

After successful completion of this unit, the students will be able to:

CO 3.1. Design and interface I/O circuits

Syllabus I/O INTERFACING

Memory Interfacing and I/O interfacing - Parallel communication interface – Serial communication interface – D/A and A/D Interface - Timer – Keyboard /display controller – Interrupt controller – DMA controller – Programming and applications Case studies: Traffic Light control, LED display , LCD display, Keyboard display interface and Alarm Controller.

UNIT -IV

Expected course outcomes:

After successful completion of this unit, the students will be able to:

CO 4.1 Design and implement 8051 microcontroller based systems

Syllabus: MICROCONTROLLER

Architecture of 8051 – Special Function Registers(SFRs) - I/O Pins Ports and Circuits - Instruction set - Addressing modes - Assembly language programming

UNIT -V

Expected course outcomes:

After successful completion of this unit, the students will be able to:

CO 5.1 Design and implement 8051 microcontroller based systems

Syllabus INTERFACING MICROCONTROLLER

Programming 8051 Timers - Serial Port Programming - Interrupts Programming – LCD & Keyboard Interfacing - ADC, DAC & Sensor Interfacing - External Memory Interface- Stepper Motor and Waveform generation - Comparison of Microprocessor, Microcontroller, PIC and ARM processors

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E. MAPPING OF CO'S WITH PO'S:

CO's/ PO's		Program Outcomes(PO's)									
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10
Course Outcomes(CO's)	CO 1.1		X					x	x		
	CO 2.1							x	x		
	CO 3.1							x	x	x	x
	CO 4.1							x	x		
	CO 5.1							x	x		

F. EXTRA SYLLABUS:

ARM processor-programming of ARM PROCESSSOR-applications

Mapping of CO's with PO's with content beyond syllabus:		Programme Outcomes (PO's)									
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10
Course Outcomes(CO's)	CO 1.1					x		x			
	CO 2.1			x							
	CO 3.1								x	x	x
	CO 4.1				x			x	x		
	CO 5.1							x	x		

G. UNITWISE PLAN

Lecture Plan for UNIT I

S. No	Topic / Portions to be Covered	Hours Required / Planned	Cumulative Hrs	Books Referred
1	Introduction to 8086	2	2	TB1
2	Microprocessor architecture	1	3	TB1
3	Addressing modes	1	4	TB1
4	Instruction set and assembler directives	2	6	TB1
5	Assembly language programming	1	7	TB1
6	Modular Programming - Linking and Relocation	1	8	TB1
7	Stacks - Procedures – Macros	1	9	TB1
8	Interrupts and interrupt service routines – Byte and String Manipulation.	2	11	TB1

Lecture Plan for UNIT II

S. No	Topic / Portions to be Covered	Hours Required / Planned	Cumulative Hrs	Books Referred
1	8086 signals	1	12	TB1
2	Basic configurations – System bus timing	1	13	TB1
3	System design using 8086	1	14	TB1
4	I/O programming	1	15	TB1
5	Introduction to Multiprogramming	2	17	TB1

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6	System Bus Structure	2	19	TB1
7	Multiprocessor configurations	1	20	TB1
8	Coprocessor	2	22	TB1
9	Closely coupled	1	23	TB1
10	loosely Coupled configurations	1	24	TB1
11	advanced processors	4	28	TB1

Lecture Plan for UNIT III

S. No	Topic / Portions to be Covered	Hours Required / Planned	Cumulative Hrs	Books Referred
1	Memory Interfacing and I/O interfacing	1	29	TB1
2	Parallel communication interface	1	30	TB1
3	Serial communication interface	1	31	TB1
4	D/A and A/D Interface	1	32	TB1
5	Timer – Keyboard /display controller	1	33	TB1
6	Interrupt controller	1	35	TB1
7	DMA controller	1	36	TB1
8	Programming and applications Case studies: Traffic Light control	1	37	TB1
9	LED display , LCD display.	1	38	TB1
10	Keyboard display interface	1	39	TB1
11	Alarm Controller.	1	40	TB1

Lecture Plan for UNIT IV

S. No	Topic / Portions to be Covered	Hours Required / Planned	Cumulative Hrs	Books Referred
1	Architecture of 8051	2	42	TB2
2	Special Function Registers(SFRs)	1	43	TB2
3	I/O Pins Ports and Circuits	1	44	TB2
4	Instruction set	2	46	TB2
5	Addressing modes	1	47	TB2

6	Assembly language programming	2	49	TB2

Lecture Plan for UNIT V

S. No	Topic / Portions to be Covered	Hours Required / Planned	Cumulative Hrs	Books Referred
1	Programming 8051 Timers	1	50	TB2
2	Serial Port Programming	1	51	TB2
3	Interrupts Programming	1	52	TB2
4	LCD & Keyboard Interfacing	1	53	TB2
5	ADC, DAC & Sensor Interfacing	1	54	TB2
6	External Memory Interface	1	55	TB2
7	StepperMotor and Waveform generation	1	56	TB2
8	Comparison of Microprocessor	1	57	TB2
9	Microcontroller	1	58	TB2
10	PIC and ARM processors	1	59	TB2

VIII. ASSESSMENT PATTERN

1. Internal assessment: 20%

As per Anna University Regulation 2017: Three tests each carrying 100 marks shall be conducted during the semester by the Department / College concerned. The total marks obtained in all tests put together out of 300, shall be proportionately reduced for 20 marks and rounded to the nearest integer (This also implies equal weight-age to all the three tests).

2. End Semester Examination: 80%

Conducted by the University.

Assessment level in Cycle – Tests and Internal assessment (%)

SL. No	Test of Knowledge level	CYCLE TESTS								IAT			Model Exam
		1	2	3	4	5	6	7	8	1	2	3	
1	Remember	20	15	10	20	20	15	10	15	15	15	10	20
2	Understand	15	25	20	10	15	25	20	15	25	25	20	15
3	Apply	10	20	25	10	10	20	10	15	20	20	10	10
4	Analyze	15	15	15	20	15	15	20	10	15	15	20	15
5	Evaluate	20	10	15	20	20	10	25	25	10	10	25	20
6	Create	20	15	15	20	20	15	15	20	15	15	15	20

COURSE IN-CHARGE

COURSE COORDINATOR

HEAD OF DEPARTMENT

IQAC COORDINATOR

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Reg. No. | A | U | H | I | P | P | O | . | C | O | M | * |

Question Paper Code : 27203

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Fourth/Fifth Semester

Computer Science and Engineering

EC 6504 — MICROPROCESSOR AND MICROCONTROLLER

(Common to Information Technology and Medical Electronics/Bio Medical Engineering/Electronics and Communication Engineering)

(Regulations 2013)

Time : Three hours

auhippo.com

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Calculate the physical address, when segment address is 1085 H and effective address is 4537 H.

2. Show how the 2 byte INT instruction can be applied for debugging.

3. What is multi programming?

4. Schematically show, how synchronization is made between 8086 and its co-processor.

5. List the operating modes of 8255 A and 8237 A.

6. What freq. transmit clock ($\overline{TxC}$) is required by an 8251 in order for it to transmit data at 4800 baud with a baud rate factor of 16?

7. Mention the number of register banks and their addresses in 8051.

8. What is the jump range?

9. Mention the features of serial port in mode 0.

10. How is A/D converter interfaced with 8051?

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PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the architecture of Intel 8086 with the help of a block diagram. (8)

(ii) Briefly describe about addressing modes of 8086. (8)

auhippo.com

(b) Explain in detail about the interrupts and interrupt service routines of 8086. (16)

12. (a) With neat diagram explain the minimum mode of operation of 8086. (16)

Or

(b) Define loosely coupled system. Explain the schemes used for establishing priority. (16)

13. (a) Draw the block diagram and explain the operations of 8251 serial communication interface. (16)

Or

(b) Draw the block diagram of programmable interrupt controller and explain its operations. (16)

14. (a) (i) Explain in detail about the Special Function Registers in 8051. (8)

(ii) Briefly explain about addressing modes of 8051. (8)

Or

(b) (i) Give PSW of 8051 and describe the use of each bit in PSW. (8)

(ii) Describe the functions of the following signals in 8051.
RST, EA, PSEN and ALE. (8)

15. (a) With a neat circuit diagram explain how a 4 × 4 keypad is interfaced with 8051 microcontroller and write 8051 ALP for keypad scanning. (16)

Or

(b) Draw the schematic for interfacing a stepper motor with 8051 microcontroller and write 8051 ALP for changing speed and direction of motor. (16)

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Reg. No. AUHIPPO.COM*

Question Paper Code : 71737

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Fourth/Fifth Semester

Electronics and Communication Engineering

EC 6504 – MICROPROCESSOR AND MICROCONTROLLER

(Common to Biomedical Engineering/Computer Science and Engineering/Medical Electronics Engineering/Information Technology)

(Regulations 2013)

Time : Three hours

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Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. The offset address of a data is (341B)H and the data segment register value is (123A)H. What is the physical address of the data?
2. Define stack register.
3. What is meant by multiprogramming?
4. Write some example for advanced processors.
5. Draw the format of read back command register, of 8254.
6. Write a 16 bit delay program in 8086.
7. Which port used as multifunction port? List the signals.
8. Illustrate the CJNE instruction.
9. List the 8051 interrupts with its priority.
10. What are the types of sensors used for interfacing?

PART B — (5 × 13 = 65 marks)

11. (a) Draw and explain the architecture of 8086 with neat diagram.

Or

(b) Describe the interrupts of 8086 and its types with service routine.

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12. (a) Explain the system bus structure of 8086. Draw the timing diagram for interrupt acknowledgement cycle.

Or

(b) Explain the closely looped configuration with neat diagram.

13. (a) Draw and explain the functional diagram of parallel communication interfacing chip.

Or

(b) Explain the need of DMA controller with its functional diagram.

14. (a) Write the available special function registers in 8051. Explain each register with its format and functions.

Or

(b) (i) Discuss the types of addressing mode with suitable example in 8051. (8)

(ii) Write an 8051 assembly language program to multiply the given number 48H and 30H. (5)

15. (a) Write a program for generation of unipolar square waveform of 1 KHz frequency using Timer0 of 8051 in mode0. Consider the system frequency as 12MHz.

Or

(b) Demonstrate the interfacing of the stepper motor with 8051 and explain its interfacing diagram and develop program to rotate the motor in clock wise direction.

PART C — (1 × 15 = 15 marks)

16. (a) Develop a 8086 based system to display the word HELLO for every 2ms in the common cathode seven segment LED display and check how many times the word displayed for one hour.

Or

(b) Develop 8051 based system design having 8Kbyte RAM to generate the triangular wave using DAC.

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Reg. No. AUHIPPO.COM*

Question Paper Code : 80345

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Fifth Semester

Electronics and Communication Engineering

EC 6504 — MICROPROCESSOR AND MICROCONTROLLER

(Common to Fifth Semester Biomedical Engineering and also common to Fourth Semester Information Technology and Medical Electronics/Computer Science and Engineering)

(Regulations 2013)

Time : Three hours

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Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the flags of 8086 microprocessor.
2. List the segment registers of 8086.
3. Define machine cycle.
4. Define Bus.
5. How DMA is initiated?
6. What is the drawback of memory mapped I/O?
7. Draw the pin diagram of 8051.
8. What is the significance of EA pin?.
9. List the modes of Timer in 8051.
10. State how baud rate is calculated for serial data transfer in mode 1.

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PART II — (5 × 16 = 80 marks)

11. (a) (i) Explain the internal hardware architecture of 8086 microprocesso with neat diagrams. (1

(ii) Write a short note about assembler directives. (

Or

(b) Explain the various addressing modes of 8086 microprocessor wit suitable examples. (1

12. (a) Discuss about the multiprocessor configurations of 8086. (1

Or

(b) Explain in detail about the system bus timing of 8086/8088. (1

13. (a) Explain in detail about DMA controller. (1

Or

(b) Explain the procedure of interfacing D/A and A/D converter circuit. (1

14. (a) Explain in detail about the architecture of 8051 microcontroller with neat diagram. (1

Or

(b) Write an ALP using 8051 instructions to receive bytes of data serial and put them in P1. Set the baud rate at 4800, 8-bit data, and 1 stop bit. (1

15. (a) Describe the different modes of operation of timers/counters in 805 microcontroller. (1

Or

(b) Draw a diagram to interface a stepper motor with 8051 microcontroller also write an 8051 ALP to run the stepper motor in both forward an reverse direction with a delay. (1

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III Year Students Details		
S.No	Reg No	Students Name
1	960120106001	Ahsan Akthar A
2	960120106002	Ganga V
3	960120106003	Ganga Devi M
4	960120106004	Makenth R
5	960120106005	Santhiya R
6	960120106006	SivaRaj S
7	960120106007	Sree Vinisha Shalini P S
8	960120106009	Thanusha T S
9	960120106303	Belwin Joshua
10	960120106305	Karthick N
11	960120106306	Sathoosh Kumar C
12	960120106307	Sneka H
13	960120106308	Sundararaj P

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QUESTION BANK

EC 8691 MICROPROCESSOR AND MICROCONTROLLER

PART A-QUESTIONS WITH ANSWERS
PART B-IMPORTANT QUESTIONS

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EC8691-MICROPROCESSOR AND MICROCONTROLLER

UNIT-I

THE 8086 MICROPROCESSOR

SYLLABUS: Introduction to 8086 – Microprocessor architecture – Addressing modes - Instruction set and assembler directives – Assembly language programming – Modular Programming - Linking and Relocation - Stacks - Procedures – Macros – Interrupts and interrupt service routines – Byte and String Manipulation.

COURSE OBJECTIVE: Know about the Architecture, addressing modes and instruction sets of 8086 Microprocessor.

PART-A

1. What is microprocessor?

A microprocessor is a multipurpose, programmable, clock-driven, register-based electronic device that reads binary information from a storage device called memory, accepts binary data as input and processes data according to those instructions, and provides result as output.

2. What is Accumulator?

The Accumulator is an 8-bit register that is part of the arithmetic/logic unit (ALU). This register is used to store 8-bit data and to perform arithmetic and logical operations. The result of an operation is stored in the accumulator. The accumulator is also identified as register A.

3. What is stack? **(EE2354April/May2013)**

The stack is a group of memory locations in the R/W memory that is used for temporary storage of binary information during the execution of a program

4. What is a subroutine program?

A subroutine is a group of instructions written separately from the main program to perform a function that occurs repeatedly in the main program. Thus subroutines avoid the repetition of same set of instructions in the main program.

5. Define addressing mode.

Addressing mode is used to specify the way in which the address of the operand is specified within the instruction.

6. Define instruction cycle.

It is defined as the time required to complete the execution of an instruction.

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KARAIKUDI

7. Write a program to add a data byte located at offset 0500H in 2000H segment to another data byte available at 0600H in the same segment and store the result at 0700H in the same segment.

MOV AX, 2000H; initialize DS with value

MOVDS, AX; 2000H

MOV AX, [500H]; Get first data byte from 0500H offset

ADD AX, [600H]; Add this to the second byte from 0600H

MOV [700H], AX; store AX in 0700H

HLT; Stop.

8. What are the different types of addressing modes of 8086 instruction set? (Nov/Dec2013) (Apr/May 2015)

The different addressing modes are:

i. Immediate

ii. Direct

iii. Register

iv. Register indirect

v. Indexed

vi. Register relative

vii. Based indexed

viii. Relative based indexed.

9. What are the different types of instructions in 8086 microprocessor? (May/jun2011)

The different types of instructions in 8086 microprocessor are:

i. Data copy / transfer instructions

ii. Arithmetic and logical instructions

iii. Branch instructions

iv. Loop instruction

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v. Machine control instruction

vi. Flag manipulation instruction

vii. Shift and rotate instruction

viii. String instruction

10. What is assembly level programming?

A program called assembler is used to convert the mnemonics of instruction and data in their equivalent object code modules. The object code modules are further converted into executab code using linker and loader programs. This type of programming is calledassembly lev programming.

11. What is a stack?

Stack is a top-down data structure, whose elements are accessed using a pointer that is implemented using the SS and SP registers. It is a LIFO data segment.

12. How is the stack top address calculated?

The stack top address is calculated using the contents of the SS and SP register. The contents of stack segment (SS) register is shifted left by four bit positions (multiplied by(0h)) and the resulted 20-bit content is added with the 16-bit offset value of the stack pointer(SP) register.

```
SS    -    5000H
SP    -    2050H
           SS    -      0101 0000 0000 0000
     10H * SS    -   0101 0000 0000 0000 0000
           SP    -      0010 0000 0101 0000
     Stack- top       0101 0010 0000 0101 0000
     Address           5    2    0    5    0
```

13. What are macros?

Macros are small routines that are used to replace strings in the program. They can have parameters passed to them, which enhances the functionality of the micro itself.

14. How are constants declared?

Constants are declared in the same way as variables, using the format:

Const–Label EQU 012h

When the constants label is encountered, the constant numeric value is exchanged for the string.

15. Write an assembly language program for a 16-bit increment and will not affect the contents of the accumulator.

```
MACRO inc16variable; Increment two bytes starting at "variable"
Local INC16 End
INC variable; Increment the low 8 bits PUSH ACC
MOV A        variable; Are the incremented low 8 bits = 0?
JNZ INC 16 End
INC variable + 1
Inc16 End;Yes–increment the upper 8 bits
POP ACC
END MAC
```

16. What will happen if a label within a macro is not declared local?

If a label within a macro is not declared local, then at assembly time, there will be two types of errors:

I. The first will state that there are multiple labels in the source.

II. The second will indicate that jump instructions don't know which one to use.

17. Write an assembly language program to load the accumulator with a constant value.

```
MACRO invert value
if (value==0)
MOV A, #1
else
clr A
end if
END MAC.
```

18. What is the difference between the microprocessor and microcontroller?

Microprocessor does not contain RAM, ROM and I/O ports on the chip. But a microcontroller contains RAM, ROM and I/O ports and a timer all on a single chip.

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19. What is assembler? **(NOV/DEC2014)**

The assembler translates the assembly language program text which is given as input to the assembler to their binary equivalents known as object code. The time required to translate the assembly code to object code is called access time. The assembler checks for syntax errors & displays them before giving the object code.

20. What is loader?

The loader copies the program into the computer's main memory at load time and begins the program execution at execution time.

21. What is linker?

A linker is a program used to join together several object files into one large object file. For large programs it is more efficient to divide the large program modules into smaller modules. Each module is individually written, tested & debugged. When all the modules work they are linked together to form a large functioning program.

22 .Explain ALIGN & ASSUME. **(Nov/Dec 2010,April/may2011)**

The ALIGN directive forces the assembler to align the next segment at an address divisible by specified divisor. The format is ALIGN number where number can be 2,4, 8 or 16. Example ALIGN 8. The ASSUME directive assigns a logical segment to a physical segment at any given time. It tells the assembler what address will be in the segment registers at execution time. Example ASSUME CS: code, DS: data, SS: stack

23. Explain PTR & GROUP

A program may contain several segments of the same type. The GROUP directive collects them under a single name so they can reside in a single segment, usually a data segment. The format is Name GROUP Seg-name,.....Seg-name PTR is used to assign a specific type to a variable or a label. It is also used to override the declared type of a variable.

24. Explain PROC & ENDP (April/May 2010)

PROC directive defines the procedures in the program. The procedure name must be unique. After PROC the term NEAR or FAR are used to specify the type of procedure. Example FACT PROC FAR.ENDP is used along with PROC and defines the end of the procedure.

25. Explain SEGMENT & ENDS

An assembly program in .EXE format consists of one or more segments. The starts of these segments are defined by SEGMENT and the end of the segment is indicated by ENDS directive. Format Name SEGMENT.

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26. Define SOP **(Nov/Dec2010)**

The segment override prefix allows the programmer to deviate from the default

Segment Eg : MOV CS: [BX] , AL

27. Define variable.

A variable is an identifier that is associated with the first byte of data item. In assembly language statement: COUNT DB 2011, COUNT is the variable.

28. What are procedures?

Procedures are a group of instructions stored as a separate program in memory and it is called from the main program whenever required. The type of procedure depends on where the procedures are stored in memory. If it is in the same code segment as that of the main program then it is a near procedure otherwise it is a far procedure.

29. Explain the linking process.

A linker is a program used to join together several object files into one large object file. The linker produces a link file which contains the binary codes for all the combined modules. It also produces a link map which contains the address information about the link files. The linker does not assign Absolute addresses but only relative address starting from zero, so the programs are relocatable& can be put anywhere in memory to be run.

30. Compare Procedure & Macro.(April/May2011)

Procedure	Macro
Accessed by CALL & RET instruction during program execution	Accessed during assembly with name to macro when defined
Machine code for instruction is put only Once in the memory	Machine code is generated for instruction each time when macro is called
With procedures less memory is required	With macro more memory is required
Parameters can be passed in registers, memory locations or stack	Parameters passed as part of statement Which calls macro

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31. What is the maximum memory size that can be addressed by 8086? (April/May 2014) (Nov/Dec 2014)

In 8086, a memory location is addressed by 20 bit address and the address bus is 20 bit address and the address bus is 20 bits. So it can address up to one megabyte (2^{20}) of memory space.

32. How many data lines and address lines are available in 8086?

Address lines= 20 bit address bus

Data lines= 16 bit data bus

33. What information is conveyed when Qs1 and Qs0 are 01?

Qs1 and Qs0 are output signals that reflect the status of the instruction queue. When Qs1 and Qs0 are 01 , then queue has first byte of an opcode.

34. What is the addressing mode of MOV AX, 55H (BX) (SI) ?

MOV AX, 55H (BX) (SI) – Base Indexed memory addressing mode.

35. What are the 8086 interrupt types?(Apr/May 2015)

Dedicated interrupts

- Type 0: Divide by zero interrupt
- Type 1: Single step interrupt
- Type 2:Nonmaskable interrupt
- Type 3: Breakpoint
- Type 4: Overflow interrupt

Software interrupts: Type 0-255

36. What is interrupt service routine?[NOV/DEC 2011]

Interrupt means to break the sequence of operation. While the CPU is executing a program an interrupt breaks the normal sequence of execution of instructions & diverts its execution to some other program. This program to which the control is transferred is called the interrupt service routine.

37. Calculate the physical address for fetching the next instruction to be executed, in 8086?

The physical address is obtained by appending four zeros to the content present in CS register and then adding the content of IP register with the above value .

For example, assuming the content of

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CS = 1200 H

IP = 0345 H

CS= 0001 0010 0000 0000 0000

0000 0011 0100 0101

0001 0010 0011 0100 0101 – Physical address=12345 H

38. If the execution unit generates effective address of 43A2 H and the DS register contains 4000 H. What will be the physical address generated by the BIU? What is the Maximum Size of the data segment?

Effective Address 43A2H

Physical Address 40000H

Maximum size of the DS is 2^{16}

39. Calculate the physical address, when segment address is 1085H and effective address is 4537H. **[Nov/Dec 2015]**

Segment address - 1085H

Effective address - 4537H

Physical address - 14D87H

---

40. Show how the 2 byte INT instruction can be applied for debugging. **[Nov/Dec2015]**

INT type

The INT instruction is used as a debugging and in case where single stepping provides more detail then is wanted, by inserting INT instructions at key points called break points.

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41. List the flags of 8086. [May/June 2016]

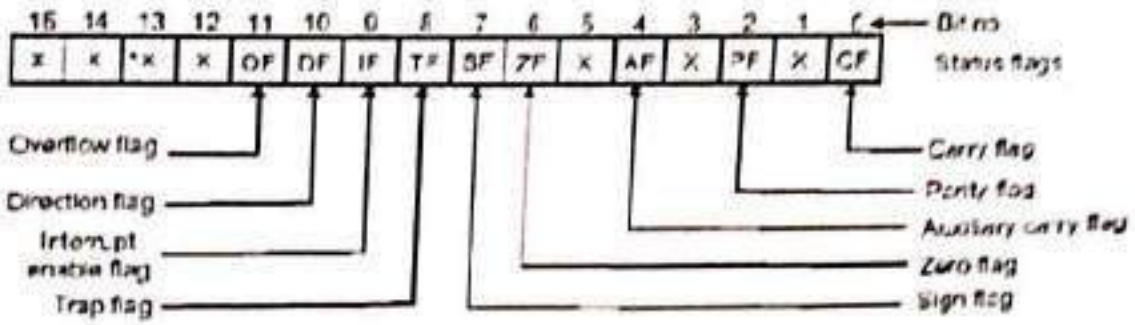

Fig.11.8: Status flags of intel 8086

- OF - Overflow Flag. Set if signed number exceeds capacity of result. ...
- DF - Direction Flag. Set by user to indicate a direction (0=forward, 1=backward) ...
- IF - Interrupt Flag. Set by user to disable hardware interrupts temporarily. ...
- TF - Trap Flag. Used by debuggers.
- SF - Sign Flag. ...
- ZF - Zero Flag. ...
- AF - Aux. ...
- PF - Parity Flag.

PART-B 4 C

1. (a) Write an assembly language program in 8086 to search the largest data in the array(6) C (April/May 2011)
   (b) Explain the various status flags in 8086. U (Nov/Dec2011)(6)

2. (a) Discuss the various addressing modes of 8086. U (April/May2011) (Nov/Dec 2014) (8)
   (b) Explain the following assembler directive in 8086 (6). U (April/May2013)(Apr/May 2015)

   i. ASSUME ii. EQU iii. DW iv. DD

3. (a)Write short notes on Macro(6) C(April/May 2012)
   (b) Explain the function of assembler directives. U(10) (April/May2011) (Nov/Dec 2014)

4. Explain the architecture of 8086. U(16) (Nov/Dec2014), (April/May2011) [Nov/Dec2015] (8)

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5. (a) Explain the register organization of 8086.U(10)(April/May2013)
(b) Explain the pin diagram of 8086 **(6) U**

6. Discuss the instruction set of 8086 in detail (8) **(April/May 2011) U**

7. Explain the interrupt and types?(8) **(Nov/Dec2010) (April/May 2011) U**

8. Explain briefly about the internal hardware architecture of 8086 microprocessor with a neatdiagram **(Apr/May 2015) (10) U**

9. Write an assembly language program in 8086 to convert BCD data – binarydata. C **(Apr/May 2015) (6)**

10. Explain briefly about Interrupt handling process in 8086. **(Apr/May 2015) (8) U**

11. Explain in detail about the interrupts and interrupt service routines of 8086. **[Apr/May 2015] [Nov/Dec 2015] U**

12. (I) Explain the Data transfer, arithmetic and branch instructions with examples.(9) U
(II) Write an 8086 ALP to find the sum of numbers in an arry of 10 element. (7) **[May/June 2016]**

13. Define interrupts and their types. Write in detail about interrupt service routine. (16) C **[May/June 2016]**

COURSE OUTCOME: Learnt the architecture, Instruction set and Programming of 8086 Microprocessor.

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UNIT-II MICROPROCESSORS AND MICROCONTROLLERS

PART A

1. ***What are the two modes in which 8086 operates?***

8086 operates in two modes

3. Minimum mode and
4. Maximum mode.

2. ***Explain the difference between minimum mode and maximum mode of operation.***

Minimum mode	Maximum mode
1. When 8086 is operating in minimum mode the pin MN/MX will be connected to VCC	When 8086 is operating under maximum mode the pin MN/MX will be connected to GND.
2. It is used in single processor environment	It is used in multi processor environment

3. ***State the functions of queue status lines QS0 and QS1 in 8086 microprocessor.***

QS1	QS0	Function
0	0	Queue is in idle state
0	1	First byte of opcode has entered into the queue
1	0	Queue empty
1		Subsequent byte of opcode has entered into the queue

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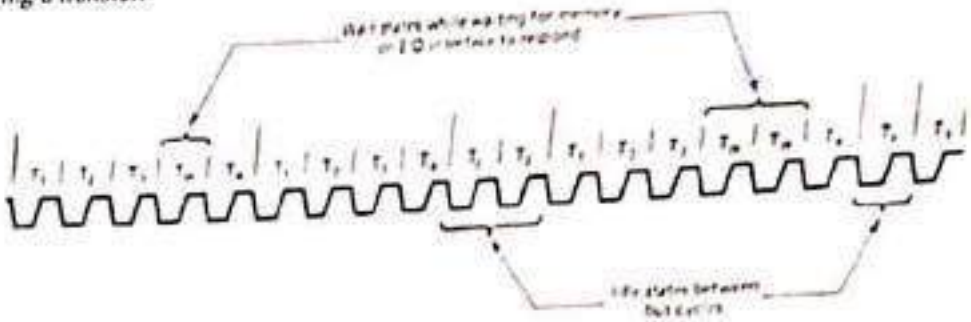
4. Define Idle cycle and wait state.

If the bus is to be inactive after the completion of a bus cycle, then the gap between successive cycles is filled with idle state clock cycles represented by T_i. Wait states are inserted between T_3 and T_4 when a memory or I/O interface is not able to respond quickly enough during a transfer.



5. What are the three principal types of IO programming?

The three principal types of I/O are:

1. Programmed I/O
2. Interrupt I/O
3. Block transfers.

6. What are the ways in which the data can be transferred to or from the port?

The transfer of data to or from a port can be done in two ways.

1. To execute an instruction that causes a single byte or word to be transferred
2. To execute a sequence of instructions that causes a special system component associated with the interface to transfer a sequence of bytes or words to or from a pre designated block of memory locations.

7. What is meant by bus cycle?

The activity involved in transferring a byte or word over the system bus is called a bus cycle.

8. Define cycle stealing.

During any given bus cycle, one of the system components connected to the system bus is given control of the bus. This component is said to be the master during that cycle and the component it is communicating with is said to be the slave. The CPU with its bus control logic is normally the master, but other specially designed components can gain control of the bus by sending a bus request to the CPU. After the current bus cycle is completed the CPU will

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return a bus grant signal and the component sending the request will become the master. Taking control of the bus for a bus cycle is called cycle stealing.

9. Give the difference between uniprogramming and multiprogramming.

Uniprogramming	Multiprogramming
1. When processes are executed in a serial fashion, the system is called a uniprogramming system.	When processes are executed in a time multiplexed fashion, the system is called a multiprogramming system
2. In such systems, normally only one process is stored in the memory at a time and the next process is not loaded for execution until the current one is terminated.	For a multiprogramming environment, the code for two or more processes is in memory at the same time and is executed.

10. What are the three states in process management.

1. **Running**-When the process is currently being executed by the CPU.
2. **Blocked**-When the execution of the process cannot be continued because it is waiting for an event to occur, e.g., it is waiting for the completion of an I/O operation.
3. **Ready**-When the execution of the process can be resumed any time. For example, the I/O process has been waiting has finished and the processing is able to continue.

11. Define semaphore.

A flag used to reserve a shared resource is called a semaphore and the operations of requesting and releasing the resource are commonly known as the P and V semaphore operators. If FLAG = 1 indicates that the resource is free and FLAG =0indicates it is busy.

12. Define bus and explain what is meant by internal bus and external bus.

A set of conductors used for communicating information between the components in a computer system is called a **bus**. If a bus connects two minor components within a major component (e.g., the control unit to the set of working registers within the CPU), it is called an internal bus. When a bus connects two major components, such as a CPU and an interface, it is called an external bus.

13. What is meant by multiprocessing system?

If a system includes two or more components that can execute instructions simultaneously, it is called a multiprocessing system. The added processors could be special purpose processors which are specifically designed to perform certain tasks efficiently, or other general purpose processors. For example, due to the 8086's limited data width and its lack of floating point arithmetic instructions, it requires many instructions to perform a single floating point operation.

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- *If any failure occur, it is easier and cheaper to find and replace the malfunctioning processor than it is to find and replace the failing part in a complex processor.*

14. What are the three basic configuration of multiprocessor configuration.

Multiprocessing features are provided in maximum mode to accommodate three basic configurations. They are the

1. Coprocessor configuration
2. Closely coupled configurations
3. Loosely coupled configurations.

15. What are the advantages of loosely coupled configuration?

A loosely coupled configuration provides the following advantages:

1. High system throughput can be achieved by having more than one CPU.
2. Each bus master module is an independent unit and normally resides on a separate PC board. Therefore, a bus master module can be added or removed without affecting the other modules in the system.
3. A failure in one module normally does not cause a breakdown of the entire system and the faulty module can be easily detected and, replaced.
4. Each bus master may have a local bus to access dedicated memory or I/O devices so that a greater degree of parallel processing can be achieved.

16. What are the three schemes that are used for establishing priority in loosely coupled configuration? (or) State the ways by which bus contention problem can be removed.

There are three schemes for establishing priority:

1. Daisy chaining
2. Polling
3. Independent requesting.

PART B

1. **With necessary diagram explain in detail about multiprocessor configuration?**
2. **Describe the maximum mode signals, and maximum mode system configuration of 8086 microprocessor in detail.(16)**
3. **Describe the minimum mode signals, and minimum mode system configuration of 8086 microprocessor in detail.(16)**
4. **Explain maximum mode bus cycle in 8086 microprocessor. (8)**

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PART B & C

1. Discuss the maximum mode configuration of 8086 by with a neat diagram.Mention the functions of the various signals.**(Apr/May 2015,Apr/May 2018)(Understand)**
2. Explain in detail about the system bus timing of 8086.**(May/June 2016, NOV/DEC 2016, APRIL/MAY 2017)(Understand)**
3. Explain the multiprocessor configuration of 8086. **(Nov07,May 07, NOV/DEC 2016, Apr/May 2018) (Understand)**
4. Explain the architecture of 8087 with neat block diagram. **(May07, May08, May10, May 12, Nov 11)(Understand)**
5. Explain the 8087 co-processor data format.**(May10,May21,Nov10) (Understand)**
6. Explain the architecture of 8089 with neat block diagram.(May 07, May 10, May 12, May 14) (Understand)
7. Explain in detail about closely coupled and loosely coupled configuration. What are the relative advantages and disadvantages? **(Nov 07,Nov 10,May 08,Nov 11)(Understand)**
8. Compare closely coupled configuration with loosely coupled configuration.**(Apr/May 2015)** / Distinguish between closely coupled and loosely coupled multiprocessor configuration**(Nov /Dec 2018)[Nov/Dec 2021) (Analyze)**
9. Discuss the schemes used to solve bus arbitration problem in multiprocessors.
10. Explain the exception handling feature of 8087. **(Nov/Dec 10)(Understand)**
11. Explain the closely coupled configuration of multiprocessor configuration withsuitableexample.**(May2014,APRIL/MAY2017(Understand)**
12. Write a 8086 assembly language program to check whether the given string is palindrome or not. **(Apr/May2015(Create)**
13. Explain the execution steps of 8087. **(May 2014)(Understand)**
14. With neat diagram explain the minimum mode of operation of 8086 **(Nov/Dec 2015)(Understand)**
15. Define loosely coupled system. Explain the schemes used for establishing priority **(Nov/Dec 2015)(Remember)**
16. Explain the following: i. multiprocessor system ii. Coprocessor iii. Multiprogrammingiv. Semaphore**(May/June 2016)(Understand)**
17. Draw the diagram showing address demultiplexing for 8086. Explain the use of each IC in the system and relevant pins and signals. **NOV/DEC2019)(Remember)**
18. Draw the timing diagram for the "Memory Read" machine cycle of 8086. Explain the function of the relevant signals and discuss how

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each signal changes in the progress of the machine cycle.**(NOV/DEC 2019) (Understand)**

19. Explain the system bus structure of 8086. Draw the timing diagram for interrupt acknowledgement cycle. **(Nov/Dec 2017)(Understand)**
20. Explain the loosely looped configuration with neat diagram. **(Nov/Dec 2017) (Understand)**
21. What do you understand from system bus structure ? explain **(Nov/Dec 2018)(Understand)**
22. With neat block diagram , explain the architecture of 8086 in maximum mode configuration. Also explain the Bus Timing diagram for input and output transfer on a maximum mode. **(Apr / May 2019) (Understand)**
23. Explain the interrupt system based on multiple 8259 with necessary block diagram. **(Apr / May 2019)(Understand)**
24. Examine all the pins functions of 8086 processor with neat pin diagram **(Understand) (Nov/Dec 2021)**

Part – C

1. Based on what you know, how would you explain I/O processor**(Understand)**
2. Explain short notes about the advanced processors **(Understand)**

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UNIT – III I/O INTERFACING

Part – A

1. **What are the modes of operation of 8255? (Understand)**

- BSR Mode
- IO Mode
  - Mode 0
  - Mode 1
  - Mode 2

2. **List the steps in the general algorithm for ADC interfacing?(Understand)**

- Ensure the stability of analog input applied to the ADC.
- Issue start of conversion (SOC) pulse to ADC.
- Read end of conversion (EOC) signal to mark the end of conversion process.
- Read analog data output of the ADC as equivalent digital output.

3. **Give the various modes & applications of 8254 timer (or) List the six modes of operation of 8253?(Apr/May 2015, Apr/May 2018) [NOV/DEC 2021](Understand)**

- Mode 0 (Interrupt on terminal count)Mode 1 (Programmable mono-shot)
- Mode 2 (Rate generator)
- Mode 3 (Square wave generator)
- Mode 4 (Software triggered strobe)
- Mode 5 (Hardware triggered strobe)

4. **List the command words of 8259A (Understand)**

Initialization command word & Operation command word

5. **What are the operational modes of 8279?** **(Remember)**

- Input (Keyboard) mode &
- Output (Display) mode

6. **What are three modes of data transmission?** **(Remember)**

- Simplex
- Half duplex &
- Full duplex

7. **List the transfer modes of 8237?**

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(Understand)

- Single transfer mode
- Block transfer mode
- Demand transfer mode
- Cascade mode
- Memory to memory transfer

8. **List the commands that can be executed by 8237? (Understand)**
   - Clear First / Last Flip flop
   - Clear Mask Register
   - Master Clear Command

9. **List the salient features of Mode0 of 8255?** **(Remember)**
   - ✓ Two 8 bit ports (Port A and Port B) and two 4 bit ports (Port C upper and lower) are available. The two 4 bit ports can be collectively used as third 8 bit port.
   - ✓ Any port can be used as an input or output port.
   - ✓ Output ports are latched. Input ports are not latched.
   - ✓ A maximum of 4 ports are available so that overall 16 I / O configurations are possible.

10. **State the features of 8255 in Mode1?**
    (Apply)

- Group A and Group B are available for strobed data transfer.
- Each group contains one 8bit data I / O port and one 4 bit control / data port.
- 8bit data port can be either used as input or output port.
- Out of 8bit portC, PC0 – PC2 are used to generate control signals for port B, PC3 – Pc5 are used to generate control signals for port A. PC6, PC7 may be used as independent data lines.State the salient features of Mode2 of 8255? (Apply)

- Single 8 bit port in group A is available
- 8bit port is bidirectional and a 5bit control port is available.
- 3 I / O ports are available at port C, PC2 – PC0
- Inputs and outputs are both latched.
- 5 control bits of portC (PC3 – PC7) is used for generating / accepting handshake signals for the 8bit data transfer on portA.

11. **What is the disadvantage in keyboard interfacing using ports(Understand)** The disadvantage in keyboard interfacing using ports is that most of the processor time is utilized in keyboard scanning and debouncing. As a result the computational speed of the processor will be reduced.

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19. What are the control words of 8251 and what are its functions?(Analyze) The control words of 8251 are mode word and command word. The mode word informs 8251 about the baud rate, character length, parity and stop bits .The command word can be send to enable the data transmission and reception.

20. What are the information that can be obtained from the status word of 8251?(Remember)

The CPU to check the readiness of the transmitter or receiver and to check the character synchronization in synchronous reception can read the status word. It also provides information regarding various errors in the data received .The various error conditions that can be checked from the status word are the parity error, overrun error and framing error.

21. What is baud rate? **(Remember)**

The baud rate is defined at which the serial data are transmitted. Baud rate is defined as 1/(the time for a bit cell).In some systems one bit cell has one data bit, then the baud rate and bits/sec are same.

22. What are the different types of data transfer scheme? **(Understand)**

The different types of data transfer scheme are

- Synchronous u data transfer scheme.
- Asynchronous data transfer scheme
- Interrupt driven data transfer scheme.

23. What are the different types of DMA data transfer scheme? (Understand)

The different types of DMA data transfer scheme are

- Cycle stealing DMA
- Block or burst mode DMA
- Demand transfer mode DMA

24. What is the need for interrupt controller? **(Remember)**

The interrupt controller is employed to expand the interrupt inputs. It can handle the interrupt request from various devices and allow one by one to the processor.

25. List some of the features of INTEL 8259. **(Understand)**

- It manage eight interrupt request
- The interrupt vector addresses are programmable
- The priorities of interrupts are programmable.
- The interrupt can be masked or unmasked individually.

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12. What is the advantage in using INTEL 8279 for keyboard and display interfacing?

(Understand)

When 8279 is used for keyboard and display interfacing, it takes care of the entire task involved in keyboard scanning and display refreshing. Hence the processor is relieved from the task of keyboard scanning, debouncing, keyboard generation and display refreshing and the processor time can be more effectively used for computing.

13. What is a programmable peripheral device? **(Remember)**

If the functions performed by a peripheral device can be altered or changed by a program instruction, then the peripheral device is called programmable device. Usually the programmable devices will have control registers. The device can be programmed by sending control word in the prescribed format to the control register.

14. What is synchronous data transfer scheme? **(Remember)**

In synchronous data transfer scheme, the processor does not check the readiness of the device after a command have been issued for read/write operation in this scheme the processor will request the device to get ready and then read/write to the device immediately after the request.

15. What is asynchronous data transfer scheme? **(Remember)**

In asynchronous data transfer scheme, first the processor sends a request to the device for read/write operation. Then the processor keeps on polling the status of the device. Once the device is ready, the processor executes a data transfer instruction to complete the process.

16. What are the operating modes of 8255? **(Understand)**

The port of 8255 can be programmed to work in any one of the following operating modes as input or output port.

Mode-0 : simple I/O port, Mode-1 : handshake I/O port, Mode-2:bi-directional I/O port

17. What are the functions performed by port-C of 8255? **(Analyze)**

- The port-C pins are used for handshake signals.
- Port-C can be used as an 8-bit parallel I/O port in mode-0
- It can be used as two numbers of 4-bit parallel port in mode-0
- The individual pins of port-C can be set or reset for various control applications.

What is USART? (Remember)

The device which can be programmed to perform synchronous or asynchronous serial communication is called USART (Universal Synchronous Asynchronous Receiver Transmitter).The INTEL 8251 is an example of USART.

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18. What are the functions performed by INTEL 8251?

(Analyze) The INTEL 8251 is used for converting parallel data to serial or vice-versa. The data transmission or reception can be either asynchronous or synchronous. The 8251 can be used to interface MODEM and or synchronously. The 8251 can be used to interface MODEM and establish serial communication through MODEM over telephone lines.

PART B

1. Explain how D/A and A/D interfacing done with 8086 with an application. **(Apr/May 2015)** **(Apply)**
2. What is DMA? Explain the DMA based data transfer using DMA controller. **(Apr/May 2015)** **(Remember)**
3. Draw the block diagram of traffic light control system using 8086. **(Apr/May 2015)**
4. Write the algorithm & assembly language program for traffic light control system. **(Apr/May2015)** **(Create)**
5. Explain the block diagram of 8255 (PPI) in detail. **(Nov 08, Nov 05, Nov 6, May 12,May 08)[Nov/Dec 2021]** **(Understand)**
6. Explain the operating modes and control word format of 8255. **(Nov 12)** **(Apply)**
7. Explain the block diagram of 8251(serial Communication) in detail **(May 10,May 06,May07)** **(Apply)**
8. Explain the control word format of 8251. **(May 10,May 06,May 12,Nov 11)(A)**
9. Explain the block diagram of 8253(timer) with control word and also explain the operating modes with timing diagram. **(May 10, Nov 08,May 12,Nov 10,Nov 11,May 7) (May/June 2016)** **(Apply)**
10. Explain the block diagram of 8279(Keyboard/display) in detail.**(Nov 07,May 05,Nov 08,Nov 0,Nov 11,May 13)[Nov/Dec 2021)** **(Apply)**
11. Explain the block diagram of 8259(PIC) in detail.**(May 10,May 06,May 12,Nov 10,May 08,May 07,Nov 11)** **(Apply)**
12. Explain the block diagram of 8237(DMA) in detail.**(Nov 07,May 06,Nov 10,May12,May 08,May 07, May 12)** **(Apply)**
13. Draw the schematic for interfacing a stepper motor with 8085microprocessor. **(May 12)(Create)**
14. Explain in detail about the temperature control by interfacing with 8085.**(Nov 07,May 08)** **(Apply)**
15. Explain the (i) modes of operation of timer (ii) operation of interrupt controller.**(May 13)** **(Apply)**
16. Explain the parallel communication interface with the microprocessor.**(April/May 2017)(Nov 12)(Apply)**
17. Draw the functional block diagram and control word format of 8254 programmable interval timer and its mode of operation and explain. **(May 10, May 12)(Create)**
18. Explain in detail about 8257 DMA controller with a neat block diagram. **(May11) (May/June2016) /** Explain in detail about DMA controller **(Apr/May 2018)(Apply)**
19. Explain the four modes of keyboard operation in 8279. **(Nov 10)** **(Apply)**
20. Explain the mode 0 operation of programmable peripheral interface. **(May 2014)** **(Understand)**
21. Draw the block diagram and explain the operations of 8251 serial communication interface **(Nov/Dec 2015)**

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(Create)

22. Draw the block diagram of programmable interrupt controller and explain its operations **(Nov/Dec 2015)**
(Create)

23. Explain the different modes of operation of a timer. **(May 2014) (May/June 2016)**
(Understand)

24. Explain the internal architecture of 8237 Direct Memory Access controller. **(May 2014) (Nov/Dec 2016)(April/May 2017)** **(Understand)**

25. Explain the procedure of interfacing D/A and A/D converter circuit. **(NOV/DEC 2016)(Apply)**

26. Draw the block diagram of the PPI 8255 and explain the ports and modes of the chip. **(NOV/DEC 2019)**
(Remember)

27. Write a program in assembly language to set/reset the following bits of Port C. Use the BSR feature of the chip. **(NOV/DEC 2019)**
(Understand)

1) PC0 to be set
2) PC7 to be reset
3) PC1 to be set

28. Draw the connections between an ADC and 8086, using 8255 as an interface. Write a program to generate a triangular waveform using this setup. **(NOV/DEC 2019)(Remember)**

29. Draw the block diagram of the 8251 and discuss how it caters to serial communication. Write the steps in transmitting one byte of data serially. **(NOV/DEC 2019)** **(Remember)**

30. Draw and explain the functional diagram of 8251 **(Nov/Dec 2017)(Remember)**

31. Draw and explain the functional diagram of keyboard and display controller **(Nov/Dec 2017) (Remember)**

32. Draw the block diagram and explain the operations of USART **(Apr/May 2018)** **(Remember)**

33. How are D/A and A/D interfaces used ?Explain.**(Nov /Dec 2018) (Remember)**

34. What are Interrupt controller and DMA controller ? Explain **(Nov /Dec 2018)** **(Remember)**

35. Draw the Block diagram and explain the operations of 8251 serial communication interface **(Apr / May 2019)**
(Remember)

36. Explain in detail about interfacing of four LCD digits to 8086 **(Apr / May 2019)** **Remember)**

PART – C

1. Draw the block diagram of I/O interface & explain in detail **(Create)**
2. Write short notes on **(Understand)**
   (i) LED display
   (ii)LCD display
   (iii) Keyboard display interface
3. Develop a 8086 based system to display the word HELLO for every 2ms in the common cathode seven segment LED display and check how many times the word displayed for one hour. **(April/May 2017)**
(Evaluate)
4. Develop a 8086 based system with 128 RAM and 4K ROM, to display the

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word HAPPY for every 2ms in the common anode seven segment LED display. Explain the delay timings. **(Nov/Dec 2017)**
(Apply)

5. Draw and explain the block diagram of alarm controller.
(Apr/May 2018)(Understand)
6. Draw the block diagram of traffic light control system using 8086. Write the algorithm and ALP for traffic light control system. **(Apr/May 2018)[Nov/Dec 2021](Understand)**

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UNIT – IV MICROCONTROLLERS

Part – A

1. **What is microcontroller? (Remember)**

Microcontroller incorporates all the features that are found in microprocessor with the added features of in-built ROM, RAM, Parallel I/O, Serial I/O, counters and clock circuit to make a micro computer system on its own.

2. **What are the alternate functions of Port 3 in 8051 microcontroller? (Remember)**

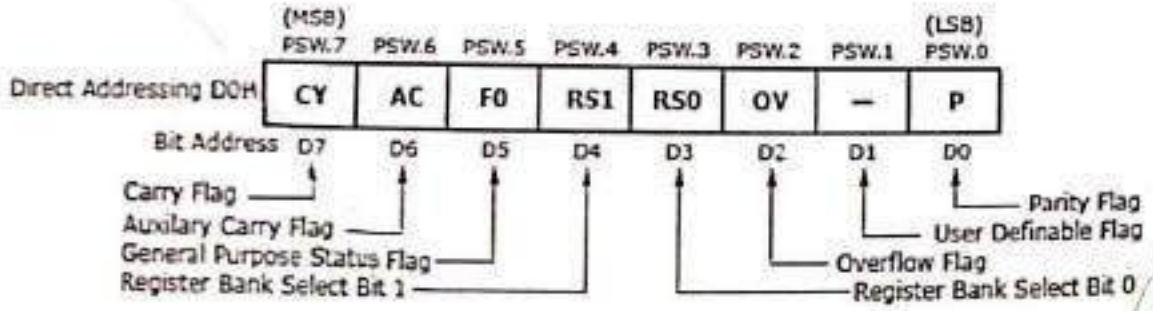
P3.0-
RXD
P3.1-
TXD
P3.2-
INT0
P3.3-
INT1
P3.4-T0
P3.5-T1
P3.6-WR
P3.7-RD

3. **What is the function of SM2 bit present in SCON register in 8051?(Remember)**

- SM2 enables the multiprocessor communication feature in modes 2 and 3. If SM2 = 1, RI will not be activated if the received 9th data bit (RB8) is 0.
- In mode 1, if SM2 = 1, RI will not be activated if a valid stop bit was not received.
- In mode 0, SM2 should be 0.

4. **Draw the diagram for processor status word (PSW) in 8051. (Apr/May 2015) [NOV/DEC 2021]**

(Understand)



5. **How do you select the register bank in 8051 microprocessor?(Apr/May 2015) (Remember)**

8051 microprocessor consists of four register banks, such as Bank0, Bank1, Bank2, Bank3 which are selected by the PSW (Program Status Word) register. These register banks are present in the internal RAM memory of the 8051 microcontroller, and are used to process the data when the microcontroller is programmed.

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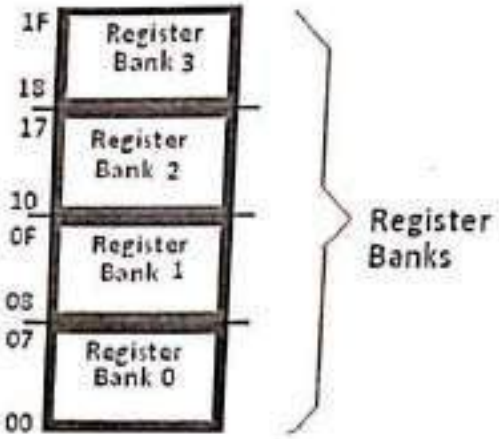

6. What is the advantage of microcontroller over microprocessor?(Remember)

- The overall system cost is low, as the peripherals are integrated in a single chip.
- The size is very small
- The system is easy to troubleshoot and maintain.
- If required additional RAM, ROM and I/O ports may be interfaced.
- The system is more reliable.

7. What is the function of IP register in 8051? (Remember)

The IP register is used to set high priority to one or more interrupts in 8051.

-	-	-	PS	PT1	PX1	PT0	PX0

Setting a bit to 1 makes the corresponding interrupt to have high priority and setting a bit to 0 makes the corresponding interrupt to have low priority.

8. Define baud rate.(Remember)

Baud rate is used to indicate the rate at which data is being transferred.
Baud rate = 1/Time for a bit cell.

9. If a 12 Mhz crystal is connected with 8051, how much is the time taken for the count in timer 0 to get incremented by one?(Remember)

Baud rate = oscillator frequency/12
$= (12 \times 10^6) / 12$
$= 1 \times 10^6 Hz$

$T = 1/f = 1/(1 \times 10^6)$
$= 1\ \mu sec$

10. What is the importance of special function registers (SFR) in 8051? (Remember)

The 8051 operations that do not use the internal 128 byte RAM address from 00 H to 7F H are done by a group of special internal registers called SPFs (Special Function Registers) which have address between 80 H and FF H.

11. Name any 4 additional hardware features available in 8051 when compared to microprocessor. (Remember)

ROM, RAM, Parallel I/O, Serial I/O, Counters, and a clock circuit are available.

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((SP)) ← (direct)

The SP is incremented by 1. The content of the indicated register is then copied to the internal RAM location addressed by SP.

POP direct: (direct) ← ((SP))

(SP) ← (SP) – 1

The content of the internal RAM location addressed by SP is read, and SP is decremented by one. The value is then transferred to the directly addressed byte indicated.

19. How does 8051 differentiate between the external and internal program memory?(Remember)

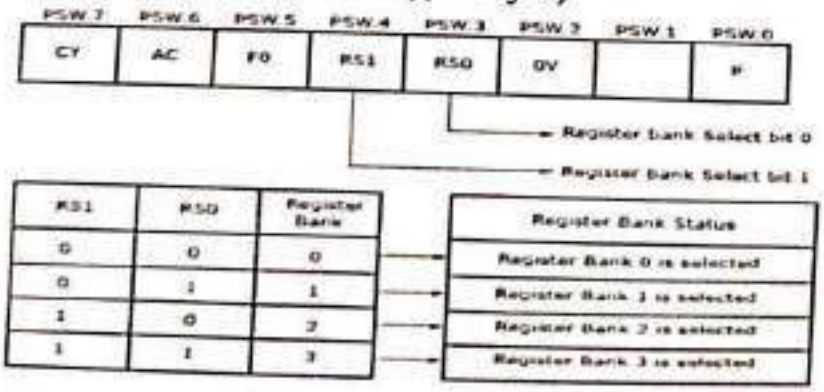
S.NO	EXTERNAL PROGRAM MEMORY	INTERNAL PROGRAM MEMORY
1	EA pin is high	EA pin is grounded
2.	PSEN signal is activated	PSEN is grounded
3.	8051 can address up to 64 KB of External program memory	4KB of internal program memory is available
4.	Accessible by only direct and indirect addressing modes	Accessible by all addressing modes

20. What are the two memory address pointers in 8051 microcontroller?

(Remember)

Program counter and Data Pointer are the two memory address pointers in 8051. The program instruction bytes are fetched from the locations in memory that are addressed by the PC. The DPTR register is made up of two 8 bit registers named DPH and DPL, which are used to furnish memory address for internal and external code access and external data access.

21. Give the PSW setting for register bank 2 as default bank in 8051 microcontroller.(Apr 2010, Apr 2013)(Analyze)



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22. What is the difference between timer and counter operation in 8051? [NOV/DEC 2021](Remember)

The timer counts the internal clock pulses whose frequency is 1/12th of oscillator frequency .The counter counts the internal clock pulses which are given through T0 pin (for counter 0) and T1 pin (for counter 1) of 8051.

reliability.

12. What is the function of DPTR register?

The data pointer register (DPTR) is the 16 bit address register that can be used to fetch any 8 bit data from the data memory space. When it is not being used for this purpose, it can be used as two eight bit registers, DPH and DPL.

13. What are the features of 8051 microcontroller?

- 8 bit CPU with registers A and B
- 16 bit PC and DPTR
- 8 bit PSW
- Internal ROM of 4KB
- Internal RAM of 128 bytes
- Two 16 bit timers and counters: T0 and T1
- Two external and three internal interrupts
  - 32 input / output pins arranged as four 8 bit ports: Port0, port1, port2 and port3.
- Control registers are: TMOD, TCON, SCON, PCON, IP and IE.

14. List any applications of microcontroller **(Remember)**

- Industrial control (process control)
- Motor speed control(stepper motor control)
- Peripheral devices(printer)
- Stand-alone devices(colour Xerox machine)
- Automobile applications(power steering)
- Home applications (washing machine)
- Length measurement
- Square wave generator

15. What is keydebouncing?(Remember)

When a key press is found, the microcontroller waits for at least 10ms before it accepts the key as input. It is called as key debouncing.

16. What is the maximum frequency of the clock signal that can be counted by 8051 counter?(Remember)

The maximum frequency of the clock signal is $1/12^{th}$ of the oscillator frequency.

17. Explain the instruction SWAP.(Understand)

SWAP instruction works only on the accumulator (SWAP A). It swaps the lower nibble and higher nibble .The lower 4 bits are put into the higher 4 bits and the higher 4 bits are put into the lower 4 bits.

E.g.- SWAP A

Beforeexecution:	**AC**	1111
	C	0000
After execution:		0000
		1111

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18. Explain the PUSH and POP instruction in 8051?(Understand)

PUSH **direct:** (sp) ← (SP) + 1

1. Explain the architecture of 8051 microcontroller with neat block diagram.**(Nov 07,May 07,Nov 05,Nov 08,Nov 06,May 06, May 08,May 12, May 2015, May/June 2016, NOV/DEC 2016, Nov/Dec 2017, Apr/May 2018][Nov/Dec 2021](Understand)**
2. Draw and explain the pin configuration of 8051.**(May 08, Nov 11) (UNDERSTAND)**
3. Explain the I/O port structure of 8051. **(May 12) (Understand)**
4. How a program and data memory is interfaced with 8051?**(May 12)(Remember)**
5. Briefly explain about 8051 addressing modes.**(Understand)**
6. Write short notes on instruction set of 8051.**(Understand)**
7. Discuss about the Special Function Registers (SFRs) of 8051.**(Create)**
8. Describe briefly various registers in 8051 microcontroller. **(May 11,Nov 11) (Evaluate)**
9. Explain the features of 8051 and compare it with 8086. **(May 11) (Understand)**
10. Describe the functions of signals present in 8051. **(May 13)(Evaluate)**
11. Draw the pin diagram of 8051 microcontroller and explain the Input / Output lines in detail. **(May 14)(Understand)**
12. Explain the TMOD function register & its timer modes of operations. **(Apr/May 2015)(Understand)**
13. Explain about Arithmetic & control instruction set in 8051. **(Apr/May 2015)[Nov/Dec 2021] (Understand)**
14. Briefly explain about addressing modes of 8051 **(Nov/Dec 2015) (APR/MAY 2017)**/ Discuss on different addressing modes of 8051 with suitable examples **(Apr/May 2018, Apr / May 2019) (Understand)**
15. Give PSW of 8051 and describe the use of each bit in PSW **(Nov/Dec 2015) (Understand)**
16. Describe the functions of the following signals in 8051. RST,EA,PSEN and ALE**(Nov/Dec 2015) (Evaluate)**
17. Write a program to bring in data in serial form & send it out in parallel form using 8051. **(Apr/May 2015) (Understand)**
18. Write an 8051 ALP to create a square wave 0f 66% duty cycle on bit 3 of port1. **(May/June 2016) (Understand)**
19. Write an ALP using 8051 instructions to receive byte of data serially and put them in PL.Set the baud rate at 4800,8-bit data, 1 stop bit. **[NOV/DEC 2016] (Understand)**
20. Write the available special function registers in 8051. Explain each register with its format and functions.**[APR/MAY 2017] (Understand)**

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21. Write an 8051 assembly language program to multiply the given number 48H and 30H.**[APR/MAY 2017](Understand)**
22. Write a program for generation of unipolar square waveform of 1 KHZ frequency using Timer 0 of 8051 in mode 0. Consider the system frequency as 12MHZ. **[APR/MAY 2017](Understand)**
23. Demonstrate the interfacing of the stepper motor with 8051 and explain its interfacing diagram and develop program to rotate the motor in clock wise direction.**[APR/MAY 2017](Understand)**
24. For 8051 microcontroller, discuss the following:
    i) How is RAM organized and addressed?
    ii)How many register banks are present in RAM and how is bank switching executed? **[NOV/DEC 2019] (Remember)**
25. Write a program in 8051 Assembly language to find the biggest of three numbers. **[NOV/DEC 2019] (Understand)**
26. Write a program in 8051 Assembly language to create a delay of 0.5 seconds, for a clock frequency of 20 MHz. (Note: Do not use any hardware timer)
    [NOV/DEC 2019] (Understand)
27. Discuss the ports and its circuits of 8051 **(Nov/Dec 2017) (Understand)**
28. What are special function registers ? explain**(Nov/Dec 2015, Nov /Dec 2018) (Understand)**
29. How input /output pins and ports help in a circuit of a microcontroller **(Nov /Dec 2018)(Understand)**
30. i) Explain in detail about the 8051 register banks and stack. **(Apr / May 2019) (Understand)**
    ii) Show the code to push R5 R6 and A onto the stack and then pop them back into R2, R3 and B , where register B = register A , R2 = R6 and R3 = R5.
    (Apr / May 2019) (Understand)
31. Briefly explain about the various addressing modes of 8051 with one example. **(Apr / May 2019)(Understand)**
32. Write a program to subtract any two 8-bit data using 8051**(Nov/Dec 2021) (Understand)**

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Part – C

Write an 8051ALP to create a square wave 66%duty cycle on bit3 of port 1. **(Understand)**

2. Write a program to bring in data in serial form and send it out in parallel form using 8051.**(Understand)**
3. How Microprocessor and microcontrollers are different from computer based controllers? **(Nov /Dec 2018) (Understand)**
4. How microprocessor and microcontroller can help to control a process or a machine tool?**(Nov /Dec 2018)(Understand)**
5. i) Discuss the number of pin sets aside for addresses in each of the following memory chips (1) 16K x 4 DRAM and (2) 16K x 4 SRAM
   ii) Briefly explain about the interfacing of 8051 with external data ROM. **(Apr/ May 2019)(Understand)**

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UNIT – V INTERFACING MICROCONTROLLER

Part – A

1. **Name the interrupts of 8051 microcontroller.**

   (Understand) External interrupt-0, External interrupt-1, Timer-0 interrupt, Timer-1 interrupt, and serial port interrupt

2. **What is the job of the TMOD register?**

   (Understand) TMOD (timer mode) register is used to set the various timer operation modes. TMOD is dedicated to the two timers (Timer0 and Timer1) and can be considered to be two duplicate 4 bit registers, each of which controls the action of one of the timers

3. **Differentiate between timers & counters. Draw the diagram of TCON in 8051. (Apr/may 2015)**

   (Analyze)

The only difference between counting and timing is the source of the clock pulses to the counters.

4. **What are the bits available in TMOD register?**

   (Remember)

GATE	C/T	M1	M0	GATE	C/T	M1	M0
TIMER 1				TIMER 0			

M1	M0	Mode
0	0	0 (13 bit Timer Mode)
0	1	1 (16 bit Timer Mode)
1	0	2 (8 bit auto reload)
1	1	3 (split Timer Mode)

GATE: Gating control when set

C/T : Timer or counter selection; 1 = counter, 0 = Timer.

5. **What are the external hardware interrupts in 8051? (Remember)**

   INT0 - External hardware interrupt 0 INT1 - External hardware interrupt 1

6. **What is the interrupt priority in 8051 and write its vector address(Remember)**

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PRIORITY	SEQUENCE INTERRUPTS	ADDRESS
Highest priority	- External interrupt - 0 (INT 0) - 0003 H	
	Timer interrupt - 0 (TF 0) - 000B H	
	External interrupt - 1 (INT 1) - 0013 H	
	Timer interrupt - 1 (TF 1) -001B H	
Lowest priority	- serial communication (RI,TI)-	0023 H

7. **When 8051 is reset, all interrupts are disabled. How to enable these interrupts?**

(Remember)

Each of the interrupts sources can be individually enabled or disabled by setting or clearing a bit in the Special Function Register IE. IE also has a global disable bit, which disables all interrupts at once.

8. **What is nested interrupts?**

(Remember) The 8051 is executing an ISR for servicing an interrupt and another interrupt occurs. If the new coming interrupt is high priority then only it can interrupt the previously occurred low priority interrupt. These are called nested interrupts.

9. **Give steps to program 8051 for serial data transfer.**

(Understand) The 8051 has a serial data communication circuit that uses register SBUF to hold data. Register SCON controls data communication, register PCON controls data rates, and pins RXD (P3.0) and TXD (P3.1) connect to serial data network.

10. **What is the significant of GATE in TMOD control register? (Remember)**

It is OR gate enable bit which controls RUN/STOP of timer 1/0. Timer/ Counter is enabled while TR 1/0 in TCON is set and signal on external interrupt INT1/0 pin is high. Cleared to 0 by program to enable timer to run, if bit TR1/0 in TCON is set.

11. **List the I/O ports available in 8051. (Remember)**

Port0 ,Port1, Port2, Port3

12. **Write down the different operating modes for serial**

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communication of 8051.
(Remember)

Serial communication of 8051 operates under four modes. They are mode 0 , mode 1, mode 2 and mode3 .SM0 and SM1 bits of SCON register specifies the mode.

13. What are the timers available in 8051? (Remember)

- Timer 0 , Timer 1

Each 16 bit timer is accessed as two separate 8 bit registers: Low byte register (TL) and High byte register (TH).

14. Compare polling and interrupt. (May/June 2016) (Understand)

In the Polling method, the microcontroller must "access by himself" the device and "ask" for the information it needs for processing. In fact we see that in the Polling method the external devices are not independent systems; they depend on the microcontroller, and only the micro is entitled to obtain access to the information it needs.

Interrupt is the signal sent to the micro to mark the event that requires immediate attention. Interrupt is "requesting" the processor to stop to perform the current program and to "make time" to execute a special code. Whenever any device needs its service, the device notifies the microcontroller by sending it an interrupt signal. Upon receiving an interrupt signal, the microcontroller interrupts whatever it is doing and serves the device.

15. Define baud rate of 8051. (May/June 2016) (Remember)

The 8051 transfers and receives data serially at many different baud rates. The baud rate in 8051 are completely programmable. This is done with help of timer 1.

16. Mention the features of serial port in mode 0 (Nov/Dec 2015) (Remember)

In mode 0, the baud rate is always the oscillator frequency divided by 12. This means if you're crystal is 11.059 Mhz, mode 0 baud rate will always be 921,583 baud.

17. List the modes of Timer in 8051. [NOC/DEC 2016]. (Remember)

Mode 0- 13-bit Timer
Mode 1- 16-bit Timer Mode 2-
8-bit Auto reload
Mode 3- Splitter Timer mode

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18. **List the 8051 interrupts with its priority.[APR/MAY 2017, Nov/Dec 2017]/Give the priority level of the interrupt sources in 8051 (Apr/May 2018) (Remember)**

Timer 0 overflow interrupt-
TF0 Timer 1 overflow
interrupt- TF1 External
hardware interrupt- INT0
External hardware interrupt-
INT1
Serial communication interrupt- RI/TI

19. **What are the types of sensors used for interfacing? [APR/MAY 2017, Apr/May 2018] (Remember)**

Temperature Sensor, IR Sensor, Ultrasonic Sensor, Touch Sensor, Proximity Sensors, Pressure Sensor, Level Sensors, Smoke and Gas Sensors.

20. **Give the format and list the function of the instruction DJNZ for 8051. (NOV/DEC 2019)(Remember)**

Function: Decrement and Jump if Not Zero

Syntax: DJNZ *register,reladdr*

DJNZ decrements the value of *register* by 1. If the initial value of *register* is 0, decrementing the value will cause it to reset to 255 (0xFF Hex). If the new value of *register* is not 0 the program will branch to the address indicated by *relative addr.* If the new value of *register* is 0 program flow continues with the instruction following the DJNZ instruction.

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Part - B

1. Describe the different modes of operation of timers/counters in 8051 with its associated register.**(Apr/May 2015)(Evaluate)**
2. How does one interface a 16 X 2 LCD display using 8051 microcontroller? **(Apr/May 2015)** **(Remember)**
3. Explain the interfacing of DAC with 8051 with neat block diagram. **(May 11, May 13)(Understand)**
4. Write an 8051 assembly language program to transfer the letter 'A' serially with 4800 baud, 1stop bit continuously.**(Understand)**
5. Explain the on-chip timer modes of 8051.**(May 10)(Understand)**
6. How to transfer data between a PC and microcontroller using serial communication?**(Remember)**
7. Draw the necessary diagrams and explain. **(Nov 12)(Understand)**
8. What is timer/counter? Explain 16-bit timer mode and 8-bit auto reload mode of 8051. **(Nov 12)(Remember)**
9. Explain how LCD and keyboard is interfaced with 8051.**(May 13)** **(Understand)**
10. Describe about serial port interface of 8051.**(May 13)** **(May/June 2016)(Remember)**
11. Explain the different techniques to convert a digital quantity into its equivalent analog quantity. **(May 2014)(Understand)**
12. With a neat circuit diagram explain how a 4 x 4 keypad is interfaced with 8051 microcontroller and write 8051 ALP for keypad scanning **(Nov/Dec 2015)(Remember)**
13. Draw the schematic for interfacing a stepper motor with 8051 microcontroller and write ALP for changing speed and direction of motor **(Nov/Dec 2015)(Understand)**
14. Draw the diagram to interface a stepper motor with 8051 microcontroller & explain. Write a 8051 assembly language program to run the stepper motor in both forward & reverse direction with delay. **(Apr/May 2015) (May/June 2016)(Understand)**
15. Describe the different modes of operation of timer/counter in 8051 microcontroller. **[NOV/DEC 2016]/** Describe the different modes of operation of timer/counters in 8051 with its associated registers **(Apr/May 2018)(Remember)**
16. Draw a diagram to interface a stepper motor with 8051 microcontroller and also write an 8051 ALP to run the stepper motor in both forward and reverse direction with address.**[NOV/DEC 2016].** **(Understand)**
17. Write a program for generation of unipolar square waveform of 1 KHZ frequency using Timer 0 of 8051 in mode 0. Consider the

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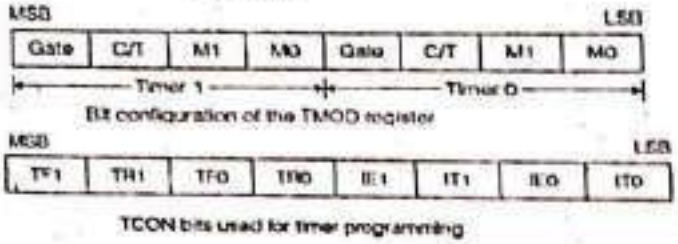
system frequency as 12MHZ. **[APR/MAY 2017].**
(Understand)

18. Demonstrate the interfacing of the stepper motor with 8051 and explain its interfacing diagram and develop program to rotate the motor in clock wise direction. **[APR/MAY 2017].**
(Understand)

19. Draw and explain the interfacing connections between an 8051 and a stepper motor by using driver IC as an interface. Write the steps and assembly program to rotate the stepper motor in the clockwise direction. **[NOV/DEC 2019]. (Understand)**

20. i) Write the assembly language program to generate a square wave using any timer, for an 8051 microcontroller.**[NOV/DEC 2019].(Understand)**

ii) For the above generated square wave, if the crystal frequency is 20 MHz and the frequency of the wave is 10KHz. Write the assembly language program referring to the bit configuration given below: **[NOV/DEC 2019] (Apply)**



TCON bits used for timer programming

21. Illustrate the serial communication in 8051 with its special function register. **(Nov/Dec 2017)(Understand)**

22. i) Interface the ADC converter with 8051 and explain with neat diagram. **(Nov/Dec 2017)(Understand)**

ii) Write the assembly language program to execute the ADC conversion.

(Nov/Dec 2017)(Apply)

23. Draw the diagram to interface a stepper motor with 8051 microcontroller and write an ALP to run the stepper motor in both forward and reverse direction with delay. **(Apr/May 2018)[Nov/Dec 2021](Apply)**

24. Write and explain what is known as serial port programming **(Nov/Dec 2018) (Understand)**

25. What are sensor interfacing and external memory interfacing? Explain **(Nov /Dec 2018) (Understand)**

26. Describe how to program and interface an LCD to an 8051 using Assembly Language Programming **(Apr / May 2019)**
(Apply)

27. Draw and explain the DAC interfacing using 8051**(Apr/May 2019)(Understand)**

28. Write a program to display a character using LCD

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display[Nov/Dec 2021]

Part – C

1. Explain about external memory interfacing to 8051 **(Evaluate)**
2. Draw and explain the ADC and DAC interfacing using 8051 **(Understand)**
3. Develop 8051 based system design having 8Kbyte RAM to generate the triangular wave using DAC. **(APR/MAY 2017). (Create)**
4. Design a microcontroller based system for taking sensor data from an agricultural field and displaying the data, generating alarms, causing actuations and also for sending the data to a PC. A complete description of this system could be given.

   The following points are to be taken care of.

   i) Draw a block diagram of the system and suggest a suitable microcontroller.
   ii)Humidity and temperature are the sensor data
   iii) Show the device that displays these parameters
   iv) If these sensor values go above a threshold, sound alarm and display should occur.
   v)If temperature goes above a threshold, a motorized pump should be activated to water the field.
   vi) Enumerate the steps for the microcontroller to be connected to the P.C

   [NOV/DEC 2019] (Create)
5. With neat block diagram explain the functions of ARM processor. Compare it with PIC and list out the major differences. **[NOV/DEC 2019](Understand)**
6. Design a circuit to generate 12MHZ frequency for a system. Write a program for generation of unipolar square waveform of 1KHz frequency using Timer 0 of 8051 in mode 0.**(Nov/Dec 2017) (Apply)**
7. i) Discuss what happens if interrupts INTO, TFO and INT1 are activated at the same time. Assume priority levels were set by the power up reset and that the external hardware interrupts are edge triggered.

   ii) With necessary diagrams explain how to interface LM35 temperature sensor and then discuss the issues of signal conditioning**(Apr / May 2019)(Under**

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V. Grango

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Part: B 100

11)

A) Architecture of 8086:-

* The 8086 cpu is divided into two independent functional parts.

Bus interface unit (BIU)

execution unit (EU)

* The 8086 the BIU interface is outside to the world. The BIU fetches read data from memory (or) ports and write data to memory or I/O ports.

* The EU receives program instruction code to the BIU memory and its executes and stored in the output them put all of its BIU.

BIU :-

* BIU contains

Stack segment (SS).

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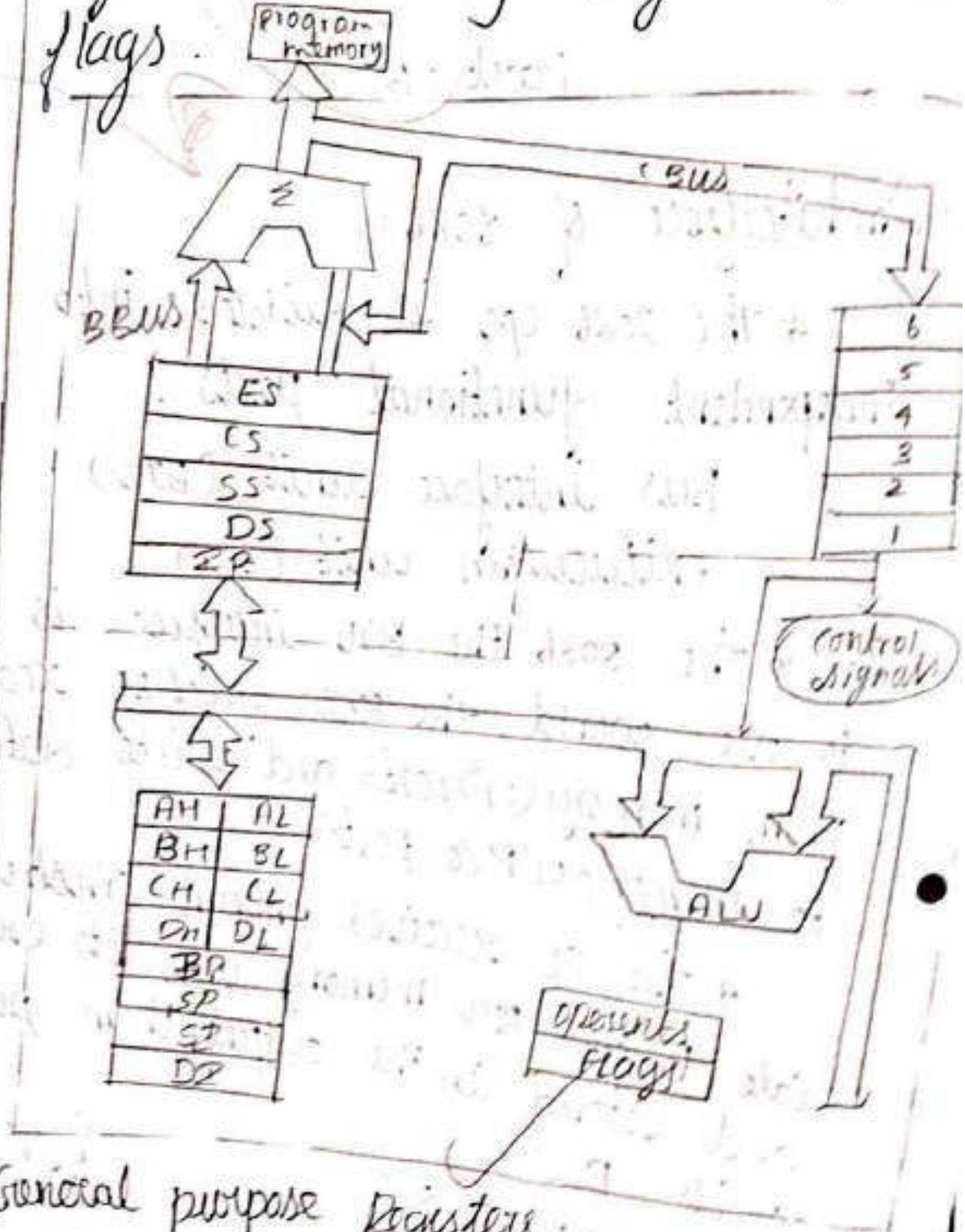
Instruction pointer, Instruction

EU :-

* EU contains ALU, general purp registers, Indexing registers, pointer flags.



General purpose Registers :-

The 16 bit general purpose registers are, AX, BX, CX, DX

Accumulator Register (AX):-

* It is a 16 bit register, consists of two 8 bit registers AL and AH.
* AL consists of low order byte of the word and AH contain high order byte.
* It is used for string manipulation.

Base Register (BX):-

* It is a 16 bit register consists of two 8 bit registers BL & BH.
* BL contain low orde byte of the word and BH contain high order byte.
* It is used for base, base indexed regis

Count Register (CX):-

* It is a 16 bit register consists of two 8 bit register CL & CH.
* CL contains low order byte of the word & CH contain high orde byte.
* It is used for counter in shift / rotate register.

Data Register (DX):-

* It is a 16 bit register consists of two 8 bit register DL & DH.

* DL contain Low order byte & DH high order byte.

Segments

* Extra segment
* code segment
* data segment
* stack segment

Code segment:-

* 16 bit register contain address of 64kb segment with processor instruction
* CS register cannot be changed directly.

Stack segment:-

* 16 bit register contain address of 64kb segment with program stack
* Stack segment register can be changed directly using pop instructions

Data segment:-

* 16 bit register contain address of 64 kB segment with program data.

* Data segment can be changed directly using pop & LDS instructions

Extra segment (ES):-

* 16 bit register contain address of 64kb segment with program data

* ES can be changed directly using pop LES instructions.

Pointers:-

Base pointers:-

* 16 bit register pointing to data from the stack segment.

Stack Pointers:-

* 16 registers pointing to the stack segment.

Source Instruction:- (SI)

* SI is a 16 bit registers.
* SI is used for base, base indexed register as well as source to the memory

Destination Instruction:- (DI)

* DI is a 16 bit registers
* DI is used for index addressing,

base & base index registers as a
Destination to the source.

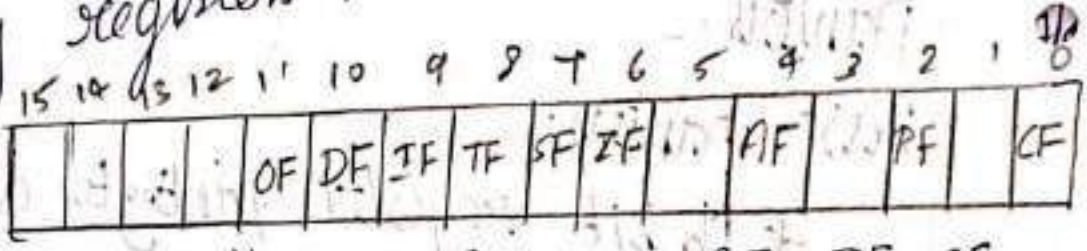
Instruction pointer:-

* It is a 16 bit register
* It is operate like a program cou

Flag registers:-

* It is a 16 bit register and nine

flag registers.



* Condition flags:- DF, SF, ZF, AF, PF, CF
* Control flags:- DF, IF, TF.

overflow flag (OF):- It is set if an overflow occurs

sign flag (SF):- It is set if an most significant bit as the result.

zero flag (ZF):- It is set if the result is zero

Auxiliary Carry flag (AF):- It is used for BCD arithmetic.

Parity flag (PF):- It is set if the most significant bit as the last result.

Carry flag (CF) :- It is set the carry or borrow occurs.
Direction flag :- It is used for ALU.
Trap flag :- It is set a trap is executed every cycle.
Internal bus flag :- It is set control the registers.

Instruction Queue :-
* Instruction Queue is first in first-out (FIFO) group of registers where 6 bytes of Instruction code is prefixed the memory.
* If the Queue is full, the BIU does not perform any Bus cycle.

ALU :-
* It is 16 bit register used to perfor Arithmetic and logical operations such as add, subtract, divide, multiply and AND, OR, XOR operations.

12

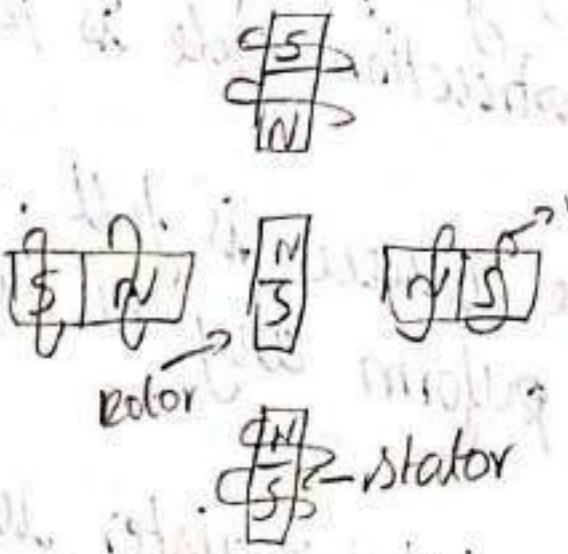
15)

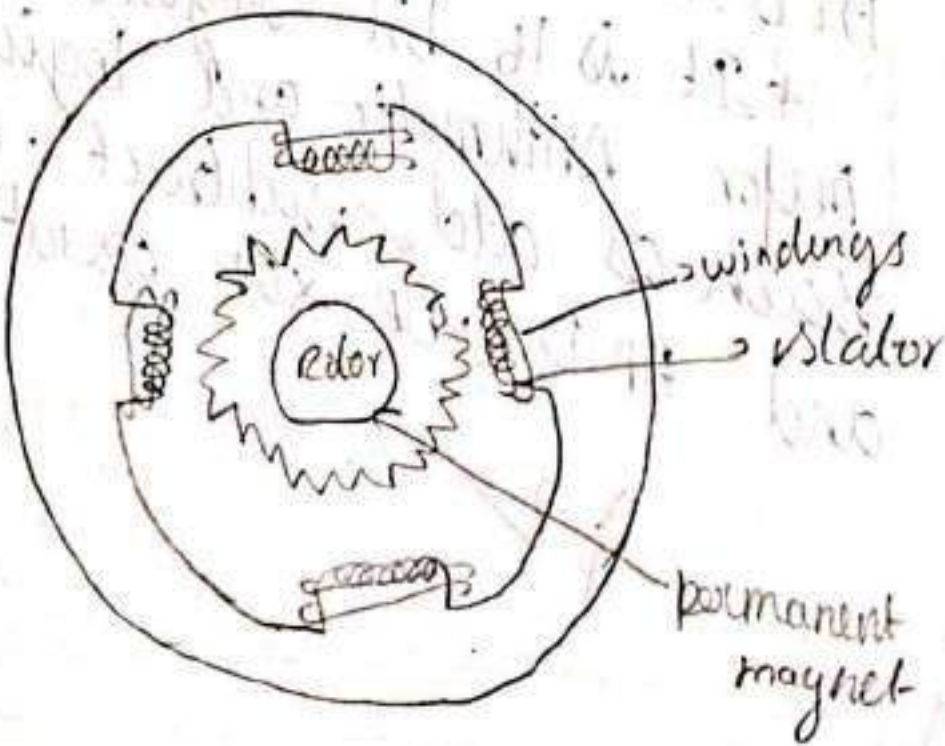
B) Stepper motor :-

* Stepper motor is a widely used device that translates electrical pulses into mechanical movement.

* Stepper motor is used to application such as, disk devices, dot matrix printers, Robotics etc.

Characteristics of stepper motor :-





* The stepper motor has a permanent magnet motor called shaft which is surrounded by the stator
* The commonly used stepper motor will have four stator windings.
* This windings are called four phase (or) unipolar windings.
* The stator is a magnet over which the electrical pulse of the coil is wound.
* One end of the coil is connected either ground (or) +5V.
* The other end of the coil is provided with fixed sequence so, the stepper motor rotates in a particular direction.
* The direction of Rotates determined by the stator poles.
* The stator poles is determined by the current pulses send through the coil.

Interfacing

step angle :-

No. of steps per revolution = $\frac{360^\circ}{\text{step angle}}$

No of steps per sec = $\frac{(\text{rpm} \times \text{no. of steps per rev})}{60}$

eg :-

step angle : 2

no. of steps per revolution = $\frac{360^\circ}{2}$

$= 180^\circ$

Switching sequence motor

two phase on :-

Step #	A	B	C	D
1	1	0	0	1
2	1	1	0	0
3	0	1	1	0
4	0	0	1	1

Clockwise ↓

Anticlockwise ↑

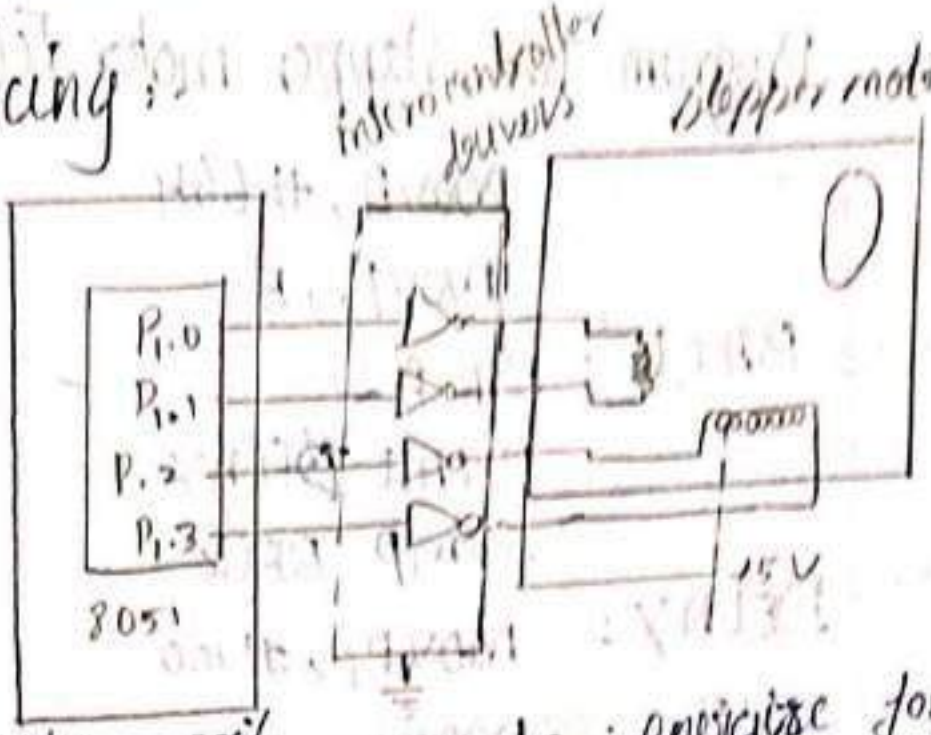
One phase on :-

Step	A	B	C	D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

Clockwise ↓

Anticlockwise ↑

Interfacing:



* The coil of stepper motor can be energize for the rotates
* It can be done the single bit of switching sequence in one end of the coil.
* The 8051 has four ports P_0, P_1, P_2, P_3
* The port P_1 namely in 8051 microcontroller is $P_{1.0}, P_{1.1}, P_{1.2}, P_{1.3}$ coce connected to the stepper motor to the drivers.
* Data '1' is send through the port to energize.
* Data '0' is send through the port to de energize.
* The 8051 microcontroller can be programmed In stepper motor to rotates clockwise direction (or) anticlockwise direction(or) both.

Program for stepper motor [clockwise

```
        MOVA, #66H
        MOVP1, A
BACK:   RRA
        ACALL DELAY
        SJMP BACK
DELAY:  MOVR1, #100
UP1:    MOVR2, #50
UP2:    DJNZ R2, UP2
        DJNZ R1, UP1
        RET
```

Program for stepper motor [anticlockwise direction

```
        MOVA, #66H
        MOVP1, A
BACK:   RLA
        ACALL DELAY
        SJMP BACK
DELAY:  MOVR1, #100
UP1:    MOVR2, #50
UP2:    DJNZ R2, UP2
        DJNZ R1, UP1
        RET
```

Minimum mode Configuration :-

* when a minimum mode pin-33 MN/$\overline{MX}$ is +5V.
* All control signals are given to the microprocessor chip itself.
* There is a single microprocessor in minimum mode configuration.
* other components are latches, transceivers, memory, clock generator and I/O ports etc.
* The latches are generally D-type flip flop like IC 8282
* It is used for separation valid address from multiplexer Address data signal.
* 3 latches are used for 20 address lines.
* The transceivers are bidirectional buffers.

* ALE is used to separate data to multiplexer address signal.

* The two buffers are bus data lines.

* The clock generator is used to generate the crystal oscillator and then it shaped and divide to more precisious.

* So, it is used to the accurate timing sequence.

* So, the timing diagram can be categorized into two parts Bus timing for read cycle, bus timing for write cycle.

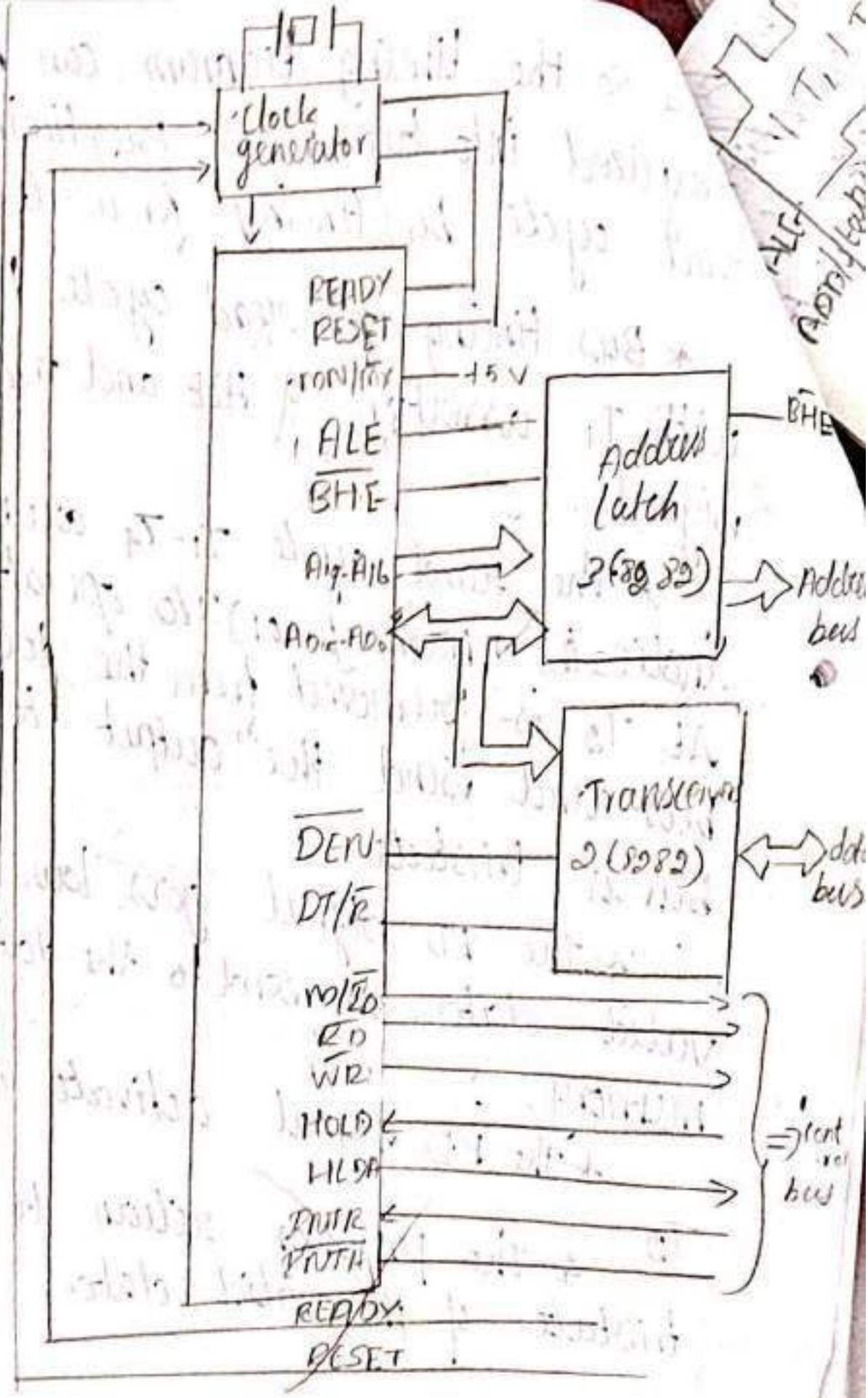
* Bus timing for read cycle begin with T_1 assertion of ALE and IO/$\overline{D}$ signals.

* The read cycle T_1-T_4 indicates memory or I/O operation. At T_3 is removed from the local data bus and send the output to the bus is tristate.

* the RD signal goes low, the valid data is send to the data memory.

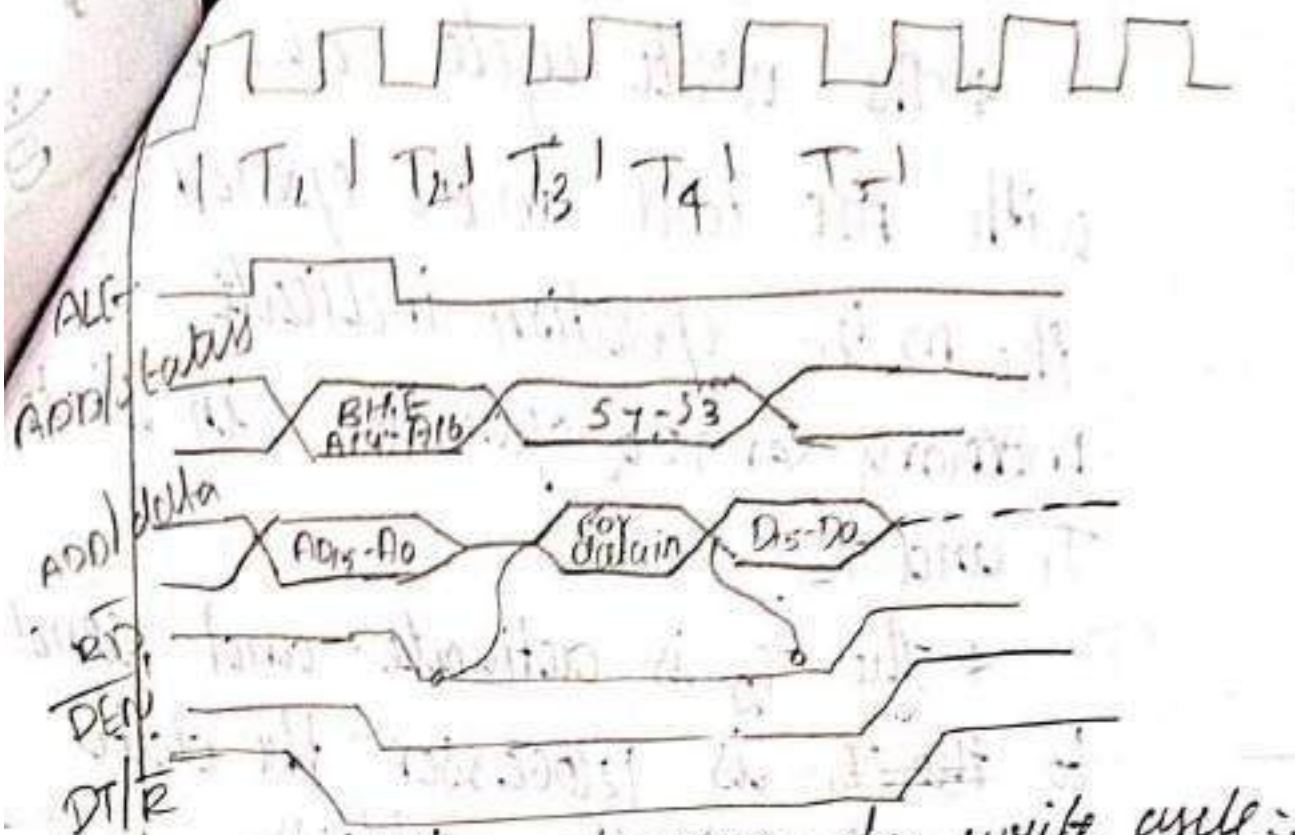
* The RD signal activate in T_3.

* The processor return to the tristate of the valid data.

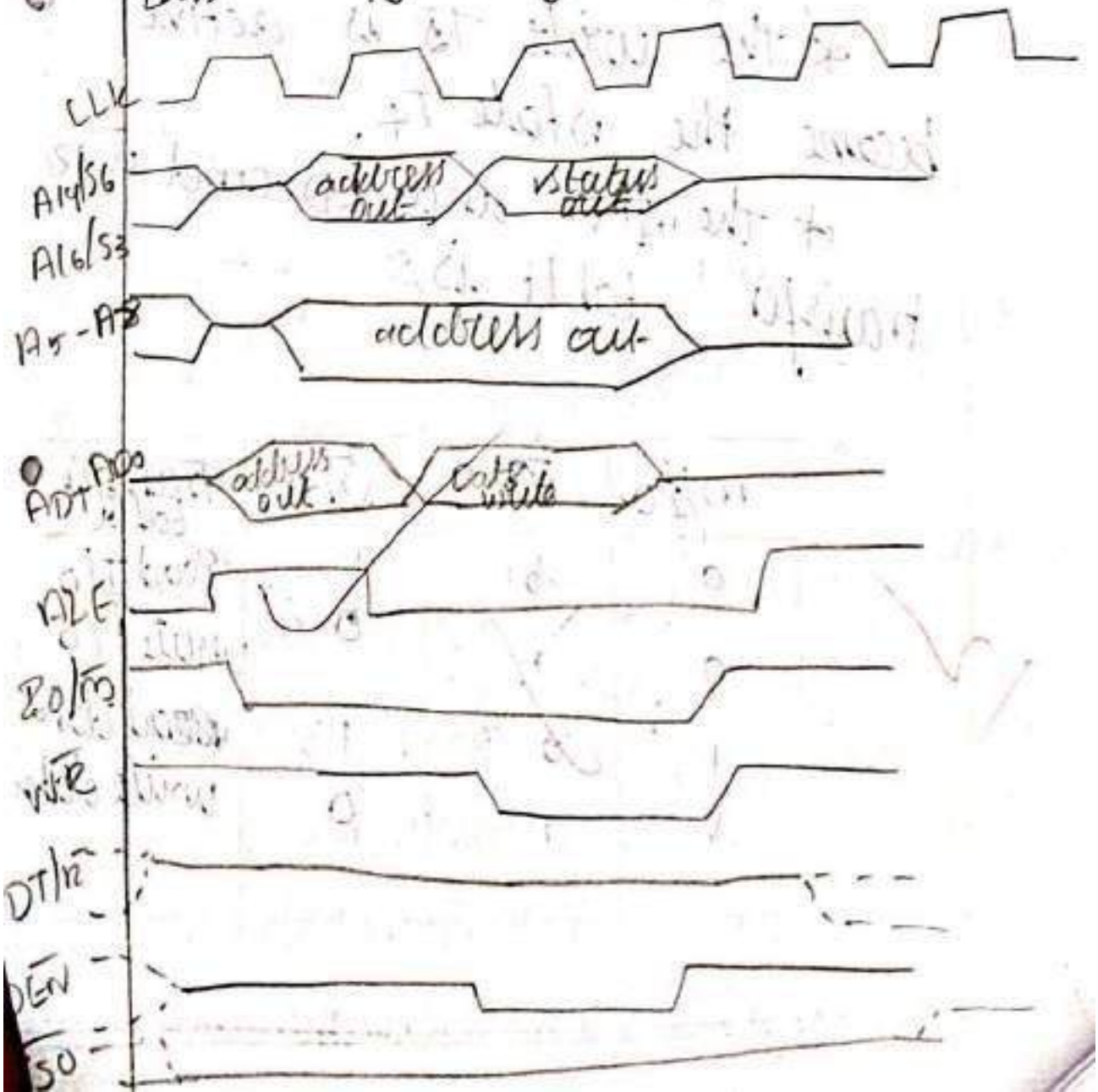


Bus Timing for minimum mode :-

* The opcode latches are read cycle for similar.



Bus timing diagram for write cycle:



* The write cycle also
with AIE and M/IO operati
the M/IO operation indicate th
memory (or) IO operation in st
T_1 and T_4.

* The T_2 is activate and st
to the T_1 is processor the data
is written to the address.

* The write T_2 is active
became the state T_4.

* the M/IO and RD and WR
transfer table is,

M/IO	RD	WR	Transfer table
0	0	1	Read I/O
0	1	0	write I/O
1	0	1	Read data
1	1	0	write data

8254 :- Programmable External timer

* RL is used for work is real life applications such that rate generator, timers and counting function.

* eg:- BCD Binary generator, generation of square wave of desired frequency & rate generation etc.

Features of 8254 :-

* 3 independent 16 bit down counters.

* 8254 can handle the input from DC 0Hz to 10mHz.

* counters can be programmed in different modes.

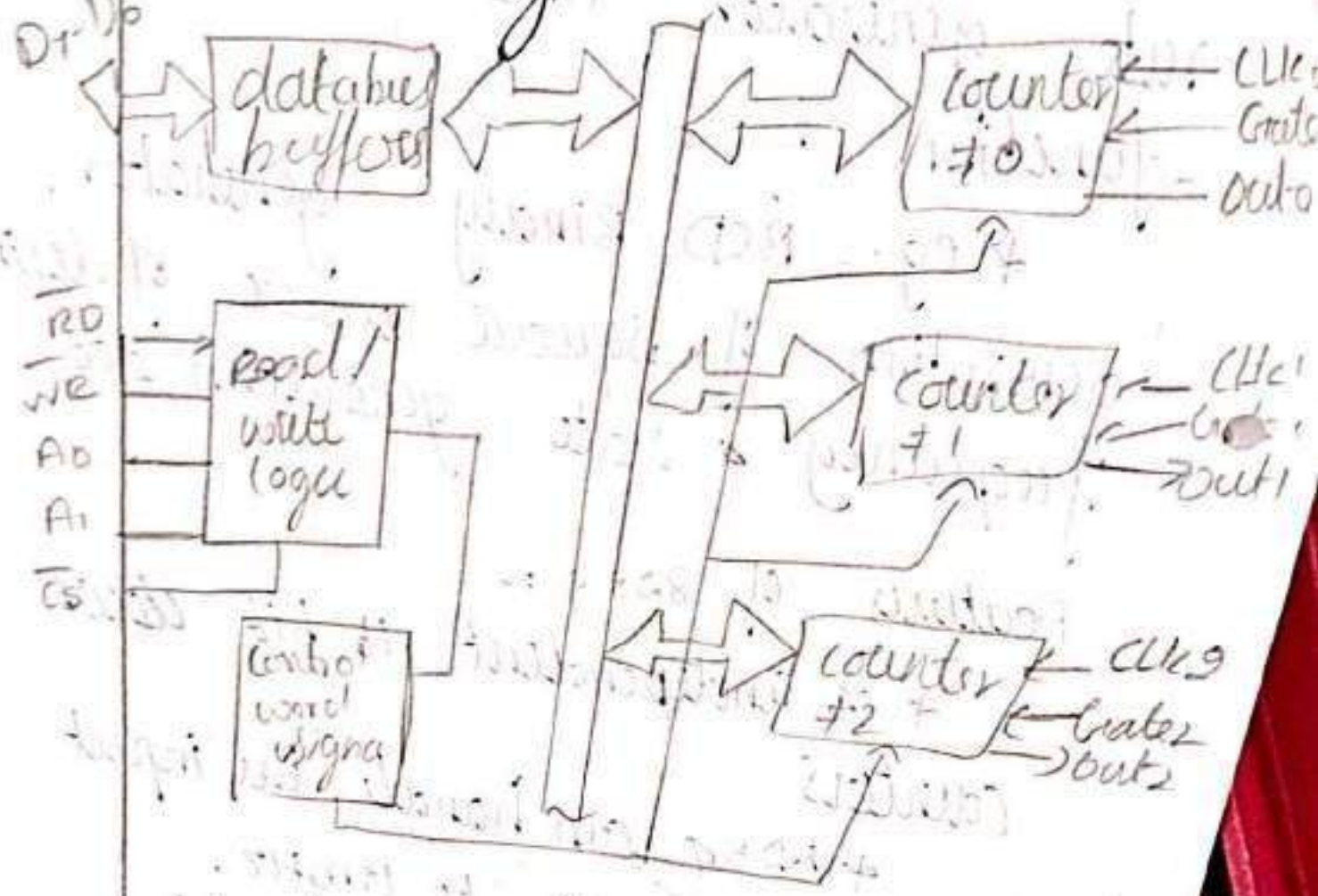
mode 0 → Interrupt on terminal count

mode 1 → programmable one-shot

mode 2 → Rate generator

mode 3 → square wave gene
mode 4 → software triggered
mode 5 → Hardware triggered

Block diagram:-



data bus buffer:-

It is a 8 bit bidirectional data buffer used to interface the 8253 to system data bus.

Read/write logic :-

* It is used to the control signal to the data bus in 8254 operation.

$\overline{CS}$	A_1	A_0	$\overline{RD}$	$\overline{WR}$	
0	0	0	0	1	Read counter 0
	0	1	0	1	read counter 1
	1	0	0	1	Read Counter 2
	0	0	1	0	write counter 0
	0	1	1	0	write counter 1
	1	0	1	0	write counter 2
	1	1	0	1	
	X	X	X	X	

Control word signal

SC_1	SC_0	RL_1	RL_0	M_2	M_1	M_0	BCD

SC -> select counter

SC_1	SC_0	operation
0	0	select counter 0
0	1	select counter 1
1	0	select counter 2
1	1	illegal

BCD -> To select character
0 -> Binary counter
1 -> Binary coded decimal counter

RL -> Rotate Load

RL_1	RL_0	operation
0	0	Read/write LSB
0	1	Read/write MSB
1	0	Read/write LSB then MSB.
1	1	

$\overline{CS}$ -> chip select
0 -> chip is selected
1 -> chip is not selected

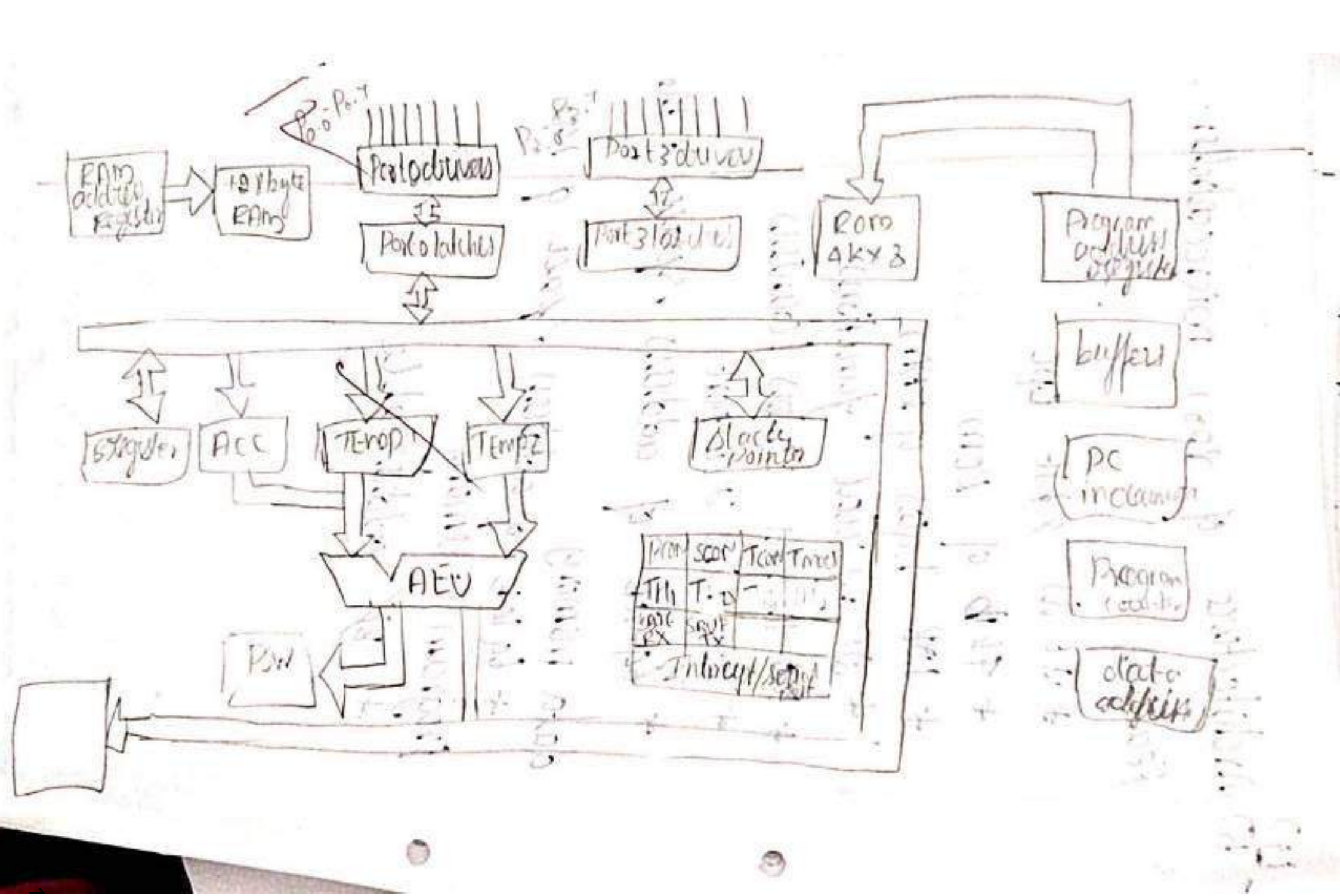
modes

modes	operation
mode 0	Interrupt on terminal count
mode 1	programmable one shot
mode 2	Rate generator
mode 3	square wave generator
mode 4	Software triggered strobe
mode 5	Hardware triggered strobe

Architecture of 8051 microcontroller :-

Features :-

* It is 8 bit CPU
* 4kB of ROM
* 128 bytes of RAM
* 21 special functions
* two 16 bits timers / counters
* 32 pins I/O port
* 64 kB of address space of the data memory
* 64 kB of address space of the program memory
* Bit addressable


Port 0 latches
Port 3 latches
ROM 4KX8
buffers
PC incrementer
Program counter
data address
Stack pointer
ACC
TEMP2
ALU
PSW
Interrupt/serial

MICROPROCESSOR AND MICROCONTROLLER

ASSIGNMENT - 4

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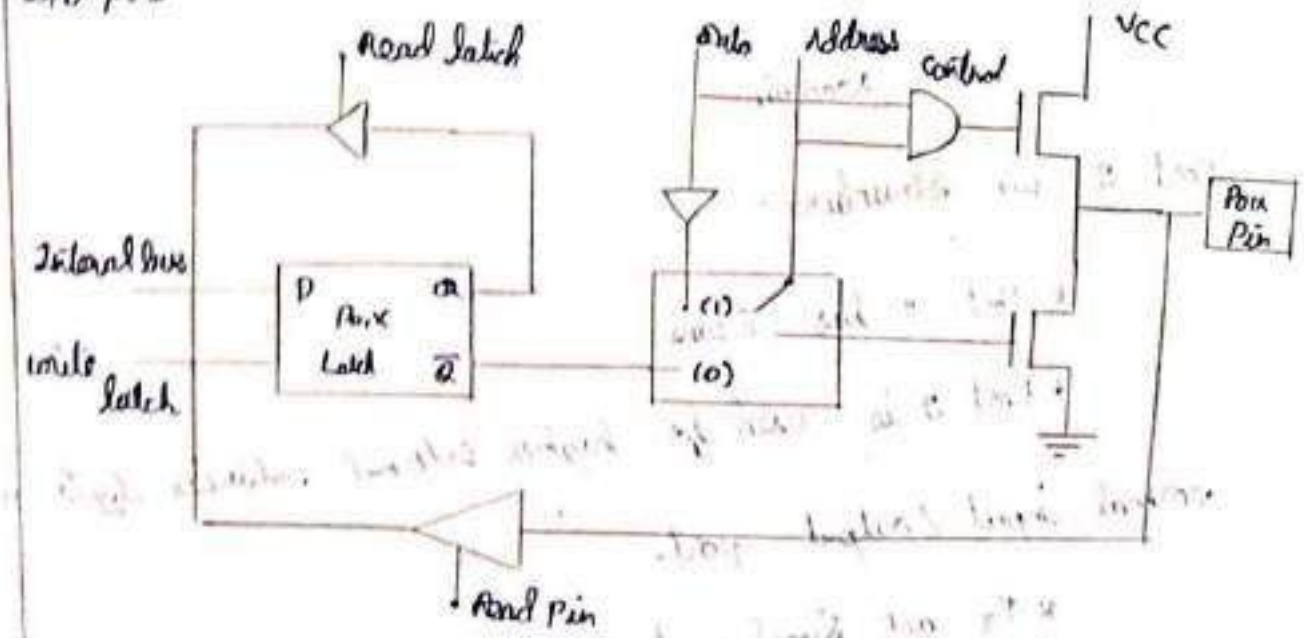
III ECE

I/O Ports Pins and Circuits:

8051 microcontroller has 4 I/O ports. Each port has 8 bits which can be used as input / output port. Total 32 I/O Pins are available. Each port has bidirectional capacity.

Port 0 pin structure:

* Port 0 has 8 pins
* Port 0 is called bidirectional port
* When control = 1, Port is used for address / data interfacing
* When control = 0, Port can be used as normal bidirectional I/O port.



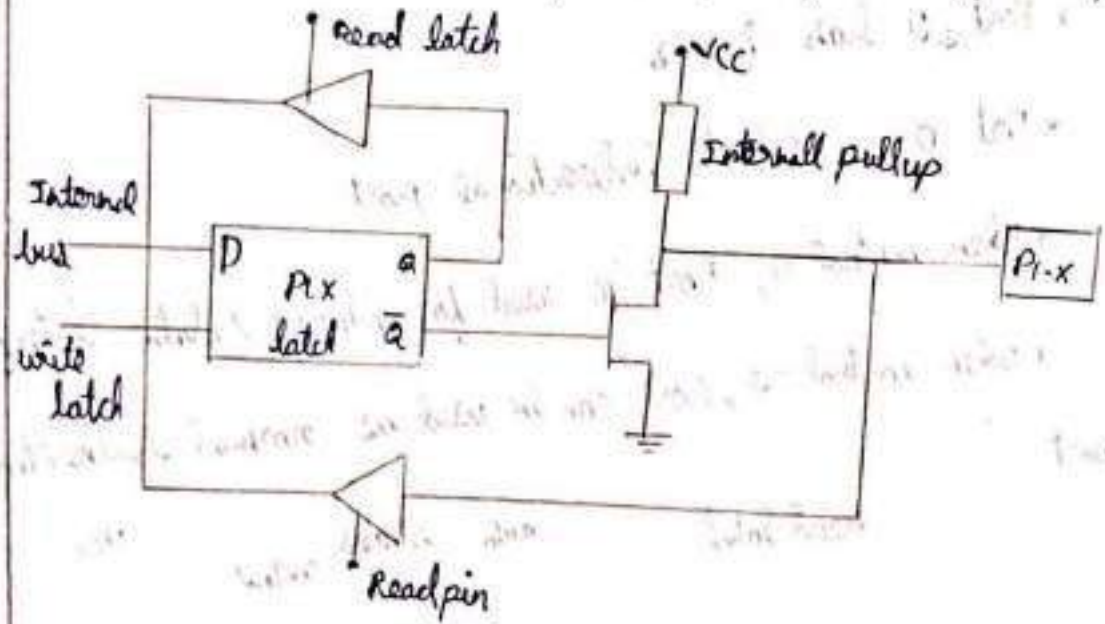
Port-1 pin structure:

* Port 1 has 8 pins (P1.0 – P1.7)

* P1 is a true I/O port, because it doesn't have any alternative function.

* It has pullup register built in

* when used as output port, the pin is pulled up (0) s



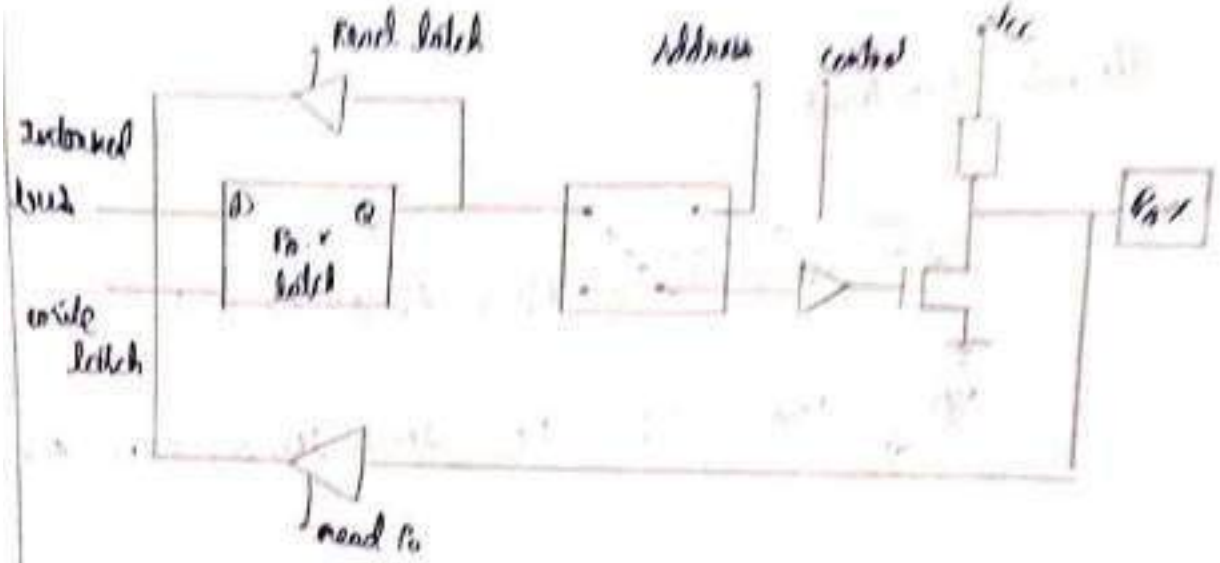
Port-2 pin structure:-

* Port 2 has 8 pins

* Port 2 is used for higher external address byte or a normal input/output port.

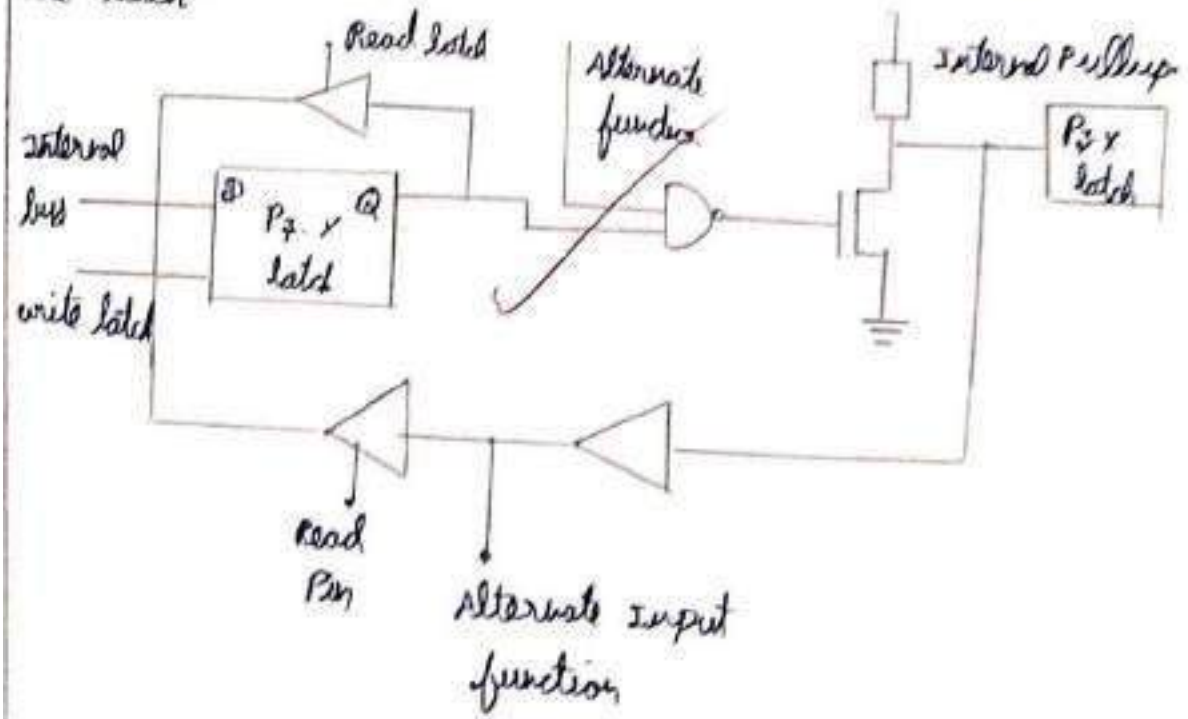
* P2 act similar to P0 when external memory is used.

* When no memory is added this port can be used as general I/O port.



Port 3 Pin structure :

* Port 3 has 8 pins
* Port 3 pins have alternate functions
* All ports can be used as general I/O also they have alternate function.
* To use the port as input port '1' should be written to the latch.



Alternate functions :-

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
RD	WR	T1	I0	INT1	INT0	TXD	RXD

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Permanent Affiliation for B.E. - Computer Science Engineering
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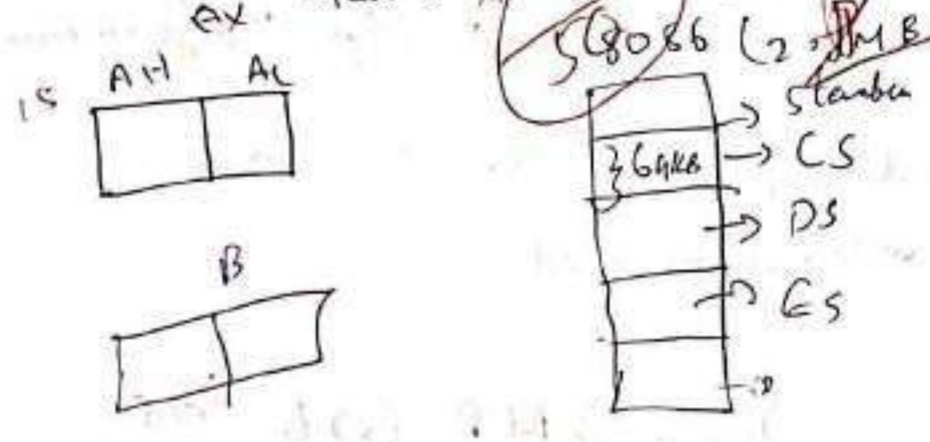
Year / Semester: III Subject Code / Title: EC 8691

Name of the Examination: Internal Exam I / II / III Total No. of Pages: 06

15/30

Part - A

1)



Format of 8086 flag register

2) linker

As we known that linker has High essential Power for the transformation of the Signal we known as the Strength of the function Signal.

3) Solution

AR 4532

Adreno 660 - Snapdragon 865+

Latest processor Snapdragon 8 gen 2.
* High Performance.

4 Opening of S1, S2, S3 Pin in Maximum mod.

Sony IMR 624 lens

S22 ultra Moon Camera

5 4 4 and 1 //

Explanation.. As we known As 8086 Hexa decimal can be carried by the A7 Cortex

Part. B

b) Architecture of 8086

The 8086 microprocessor contains of two equal units

(i) BIU
(ii) EU

BIU - Bus Interface unit

EU - Execution unit

BIU

It consists of

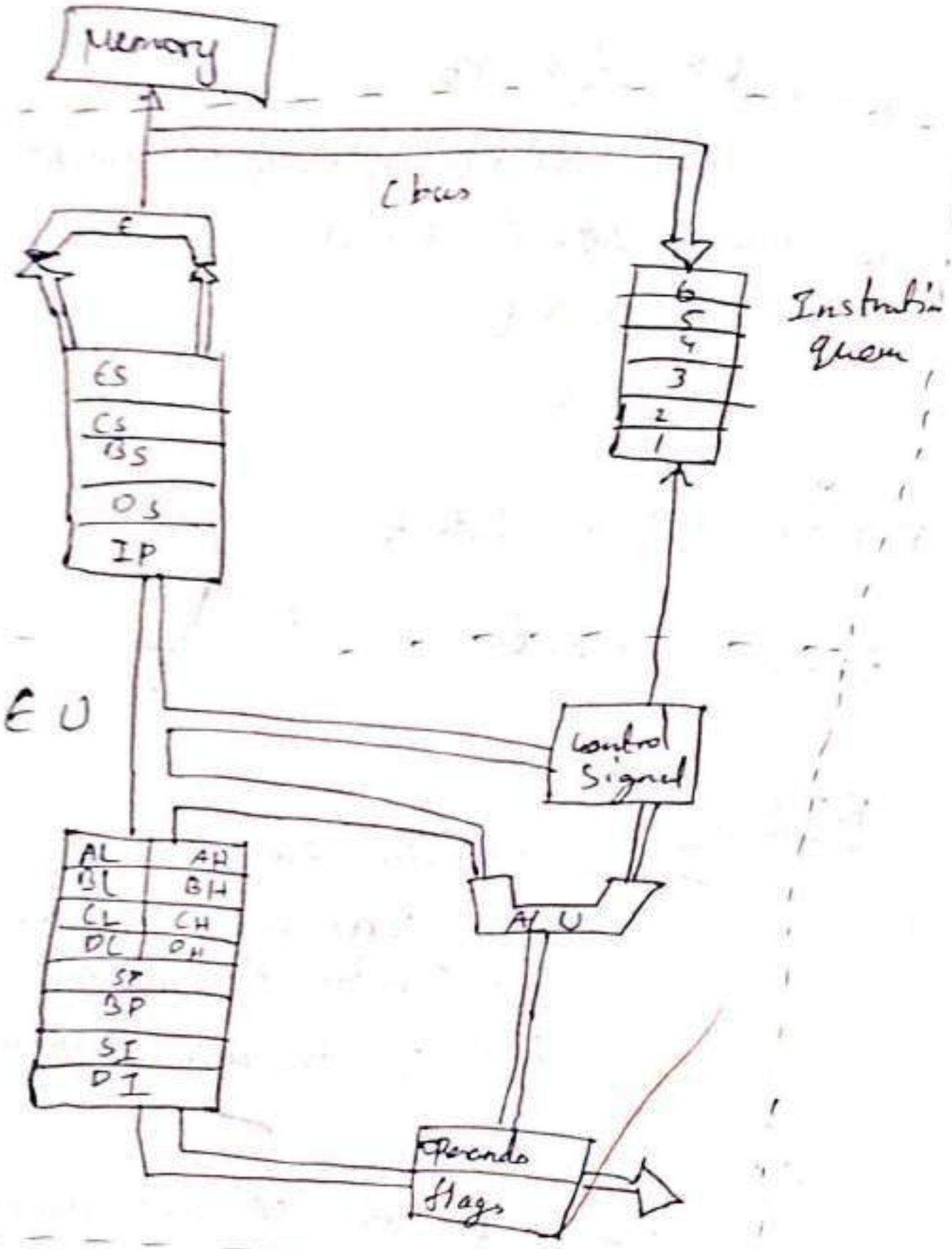
(i) Segment register
(ii) Instruction Pointer
(iii) Instruction Queue

EU

The execution of unit process the data from the bus interface units. It consists of ALU

(i) Regular purpose register
(ii) Index register
(iii) Pointer
(iv) Flag register

BIU



Internal hardware architecture of 8086 microprocessor

Construction of BIU.

The BIU is defined as the Bus Interface unit as we known the function of the data Bus Bar has been transfer from the Memory

Memory

The memory is the storage device of space to store the limited data digital or the storage for (or) Action the function on the Bus Bar.

C. Bus

The C. Bus is the signal Strength tranforming medium from several place to the

Instruction

functioning mechanism of the bios

as we know Cs register

BIT register

The BIT register is the Bit of storage device to Store the data through the Serial Spec of the Basic Junctional System

(or) ES - register

CS - register

BS - register

OS - register

IP - register

Now the Signal has been transfer to the Position of the EU.

Instruction queue

The Instruction has been stored from the register bit as we can see on the above figure.

EU - construction

The EU is defined as the Execution Unit of the process of 8086 in the Achievement of the hardware function of register and point flag register for storage Index

ALU = Arithmetic and logic Units

ALU

The ALU is the Programing language which can easily Communicate through the computer.

Control Signal

The control signal is the medium which can easily connect the input register and rectify and know the signal has been given to the Arithmatic and logic unit.

Flags

The flags are otherwise called as the operands for the operational output functions of the operating system

(4) a) Minimum mode of 8086

* The minimum pin 33 is MN/MX = 1 High

* The another part are latches, memory, clock generator, logical signal, I/O devices, transceiver.

* There is single microprocessor

* It is a Arithmetic latch enable

* It retrieve the fetched data

Catches

The seperates the address for the multiplexed data address

Transceiver

It is seperates the addres

for the multiplexed data address

Memory

The user interface memory and

Storage memory

EEPROM → It is stage memory

RAM → It is user interface memory

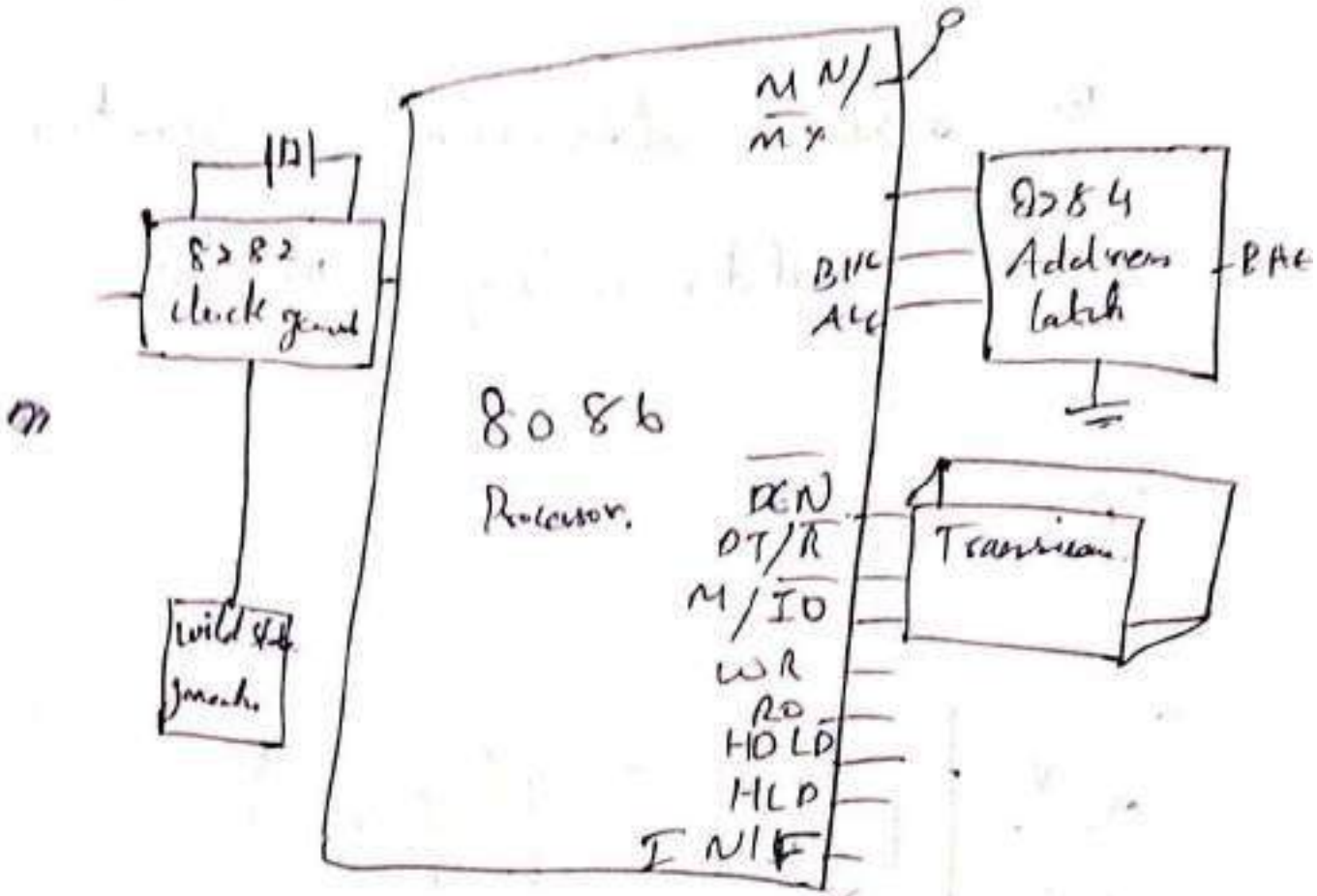
RAM → Random access Memory

Clock generator

It generates timing and clock Pulse

Minimum mode operation

of 8086



Construction

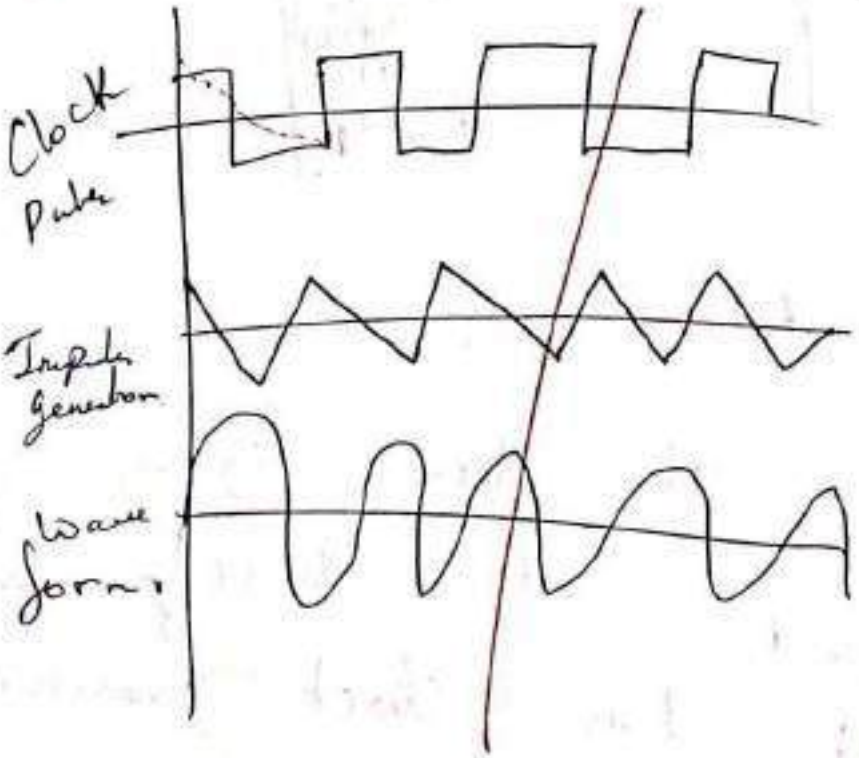
The above figure is the 8086 processor.

It has Clock generator about

It will Generate an impulse at Second time difference

Also it is connected to wired
stat impulse generator to
generate an pulse of 8254
is an addressing generator
of an addressing mode.

Pulse generator



R. Santhiya.

Class Test:

NORECO5

III Year 6 Sem

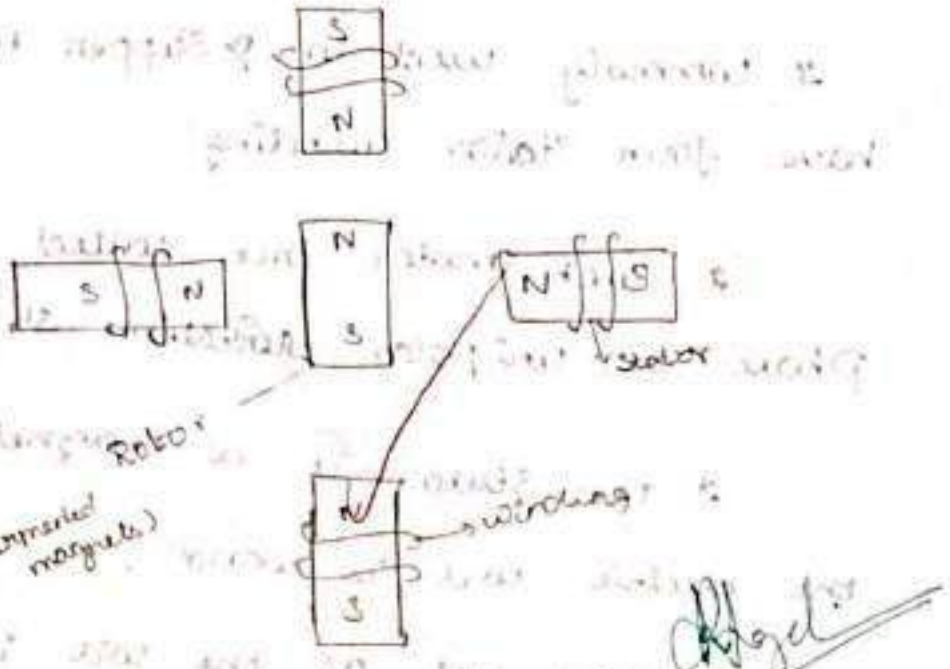
13/20

1. Stepper Motor Interfacing.

The Stepper Motor is a widely used devices it translate electrical pulse in to mechanical movement.

The stepper motor is used in application such as Disk drives, Robotics etc.

Characteristics of Stepper Motor



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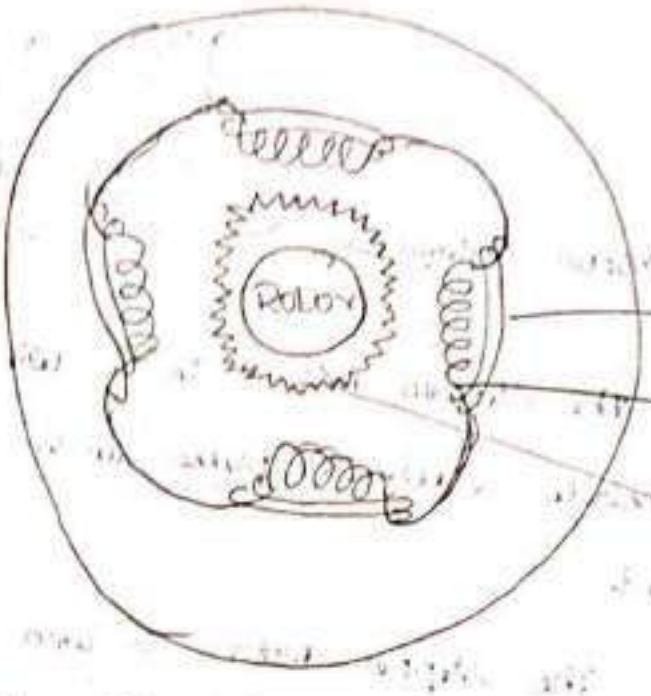


* The stepper motor is a permenent magnet Rotor called shaft. Which is surrounding by stator.

* commonly used in stepper motor will have four stator winding.

* such motor are called four phase (or) unipolar rotation stepper motor.

* The stator is a magnet over which the electric coil is wond.

* one end of the coil is connected to either ground or +5v.

* The other end of the coil is interfacing provided with a fixed coil of the winding stator.

* Direction of rotation is determined by stator poles.

* Stator phase poles are determined by the current pulse send through the coil.

Step angle.

$$\text{No. of steps per revolution} = \frac{360^\circ}{\text{step angle}}$$

$$\text{Steps per second} = \frac{\text{rpm} \times \text{steps per revolution}}{60}$$

Example.

Step angle = 2

$$\text{No. of steps per revolution} = \frac{360^\circ}{2}$$

$$= 180 \text{ steps}$$

Switching sequence of Motor.

Full step. Two phase on.

Stator winding

Step #	A	B	C	D
1	1	0	0	1
2	1	1	0	0
3	0	1	1	0

Anticlock wise

Clock wise

One phase ON

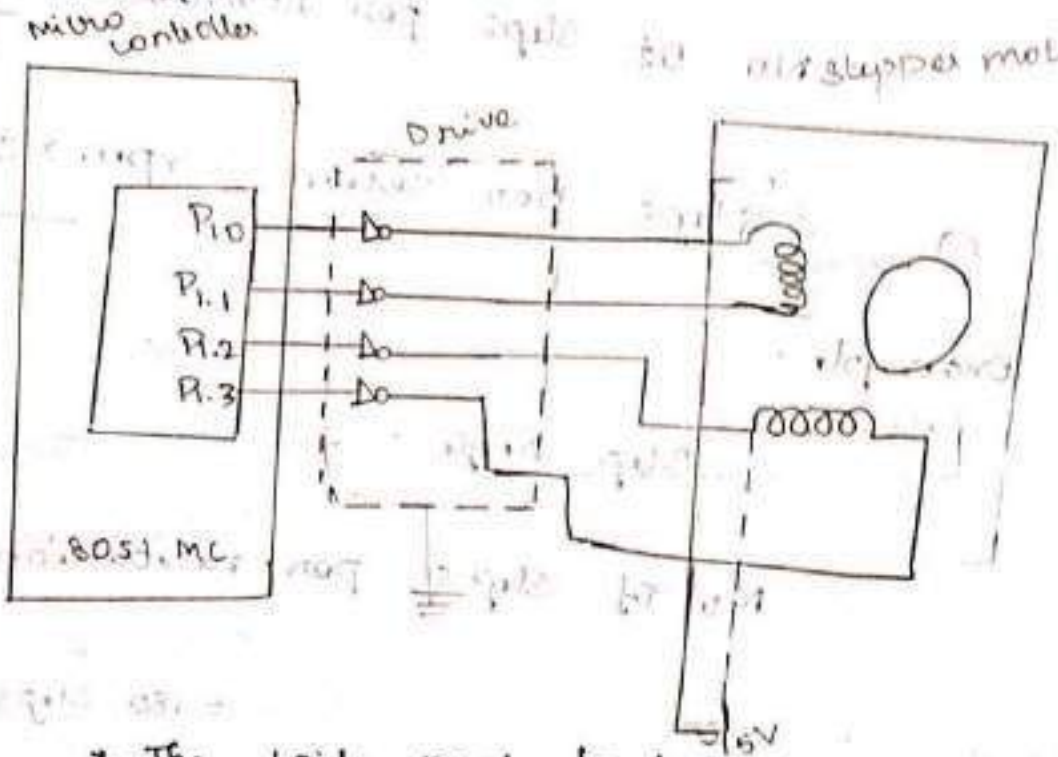
Stator winding

Step #	A	B	C	D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

Clock wise

Anti clock wise

Interfacing .



* The coils need to be energized for the rotation

* This can be done by sending a bit sequence to one end of the coil.

* The bit sequence will make one coil phase on (or) two phase ON

* The microcontroller 8051 has four I/O ports P_0, P_1, P_2, P_3

* The four pins from port 1 of 8051 namely $P_{1.0}$, $P_{1.1}$, $P_{1.2}$, $P_{1.3}$ are connected to the stator windings by the driver

* We can program the microcontroller of 8051 sending electrical pulse into the winding of the stator.

* Data '1' is send through the port to energized the coil.

* Data '0' is send through the port of de-energize the coil.

* The 8051 Microcontroller has Programmed to stator. Rotate the Stepper motor in the clock wise direction and the anti-clock wise directions.

Programmed

Program: [Using one location]

```
        MOV A, #66H
        MOV P1, A
BACK:   RLC A
        ACALL DELAY
        SJMP BACK

DELAY:  MOV R1, #100H
UP1:    MOV R2, #50H
UP2:    DJNZ R2, UP2
        DJNZ R1, UP1
        RET
```

Program: [For using one location]

```
        MOV A, #66H
        MOV P1, A
BACK:   RLC A
        ACALL DELAY
        SJMP BACK

DELAY:  MOV R1, #100H
UP1:    MOV R2, #50H
UP2:    DJNZ R2, UP2
        DJNZ R1, UP1
        RET
```

Thanusha T.S.
III ECE
Class Test
MPMC
3ORECO9

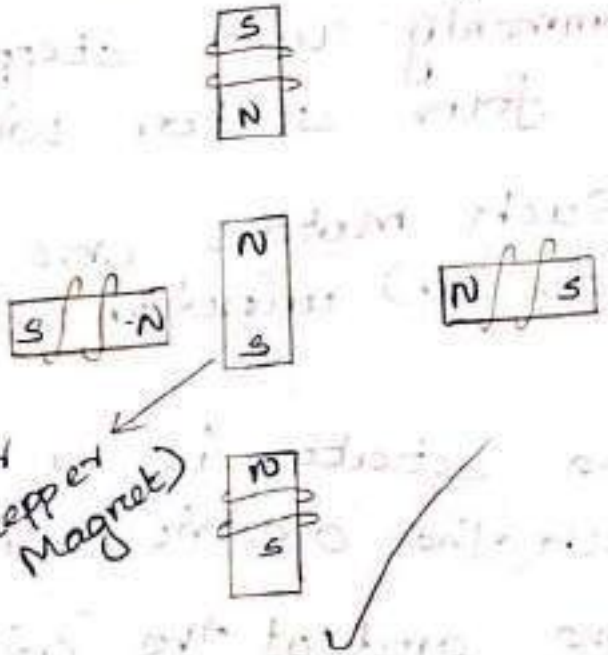
15/20

Stepper Motor Interfacing

A stepper motor is a widely used device that translate Electrical pulses into mechanical moment

A stepper motor is used in application such as disk drives, dot matrix printers, Robotics, etc

Characteristics of Stepper Motor



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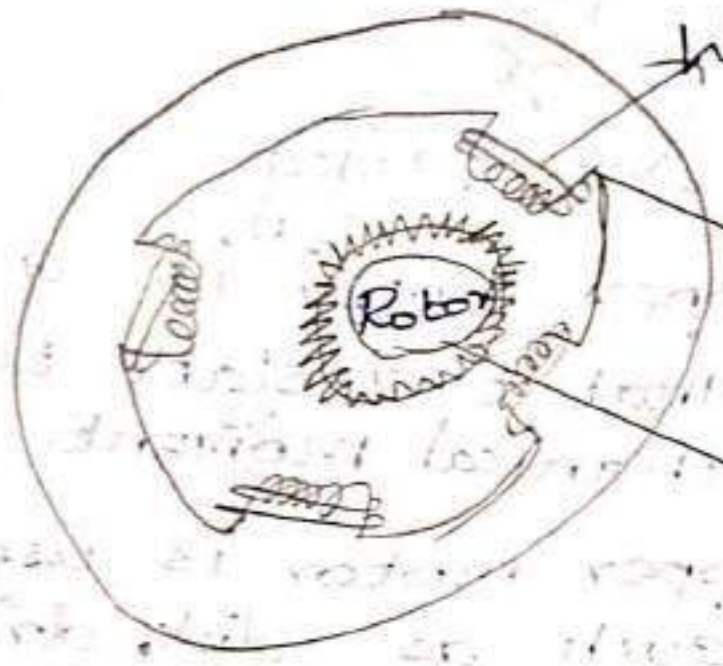


A stepper has a permanent magnet rotor called shaft which is surrounded by the stator

Commonly used stepper motor will have four stator winding

Such motors are called four phase (or) unipolar stepper winding.

The stator is a magnet over which the electric coil is wound

One end of the coil is connected to either ground or +5V

The other end of the coil is provided with a fixed sequence. So that stepper motor rotate

a particular direction

Direction of rotation is determined by the stator poles

Stator poles are determined by the current pulse send through the coil

Step angle

No. of step per revolution = $\frac{360^\circ}{\text{step angle}}$

Total steps per second

= $\frac{(\text{rpm} \times \text{steps per revolution})}{60}$

Eg:

Step angle = 2°

No. of step per revolution = $\frac{360}{2}$

= 180 step

Switching motors of Stepper

Full step: Two phase on

Stator winding

Step#	A	B	C	D
1	1	0	0	1
2	1	1	0	0
3	0	1	1	0
4	0	0	1	1

Clock wise

Anti clock wise

One phase ON

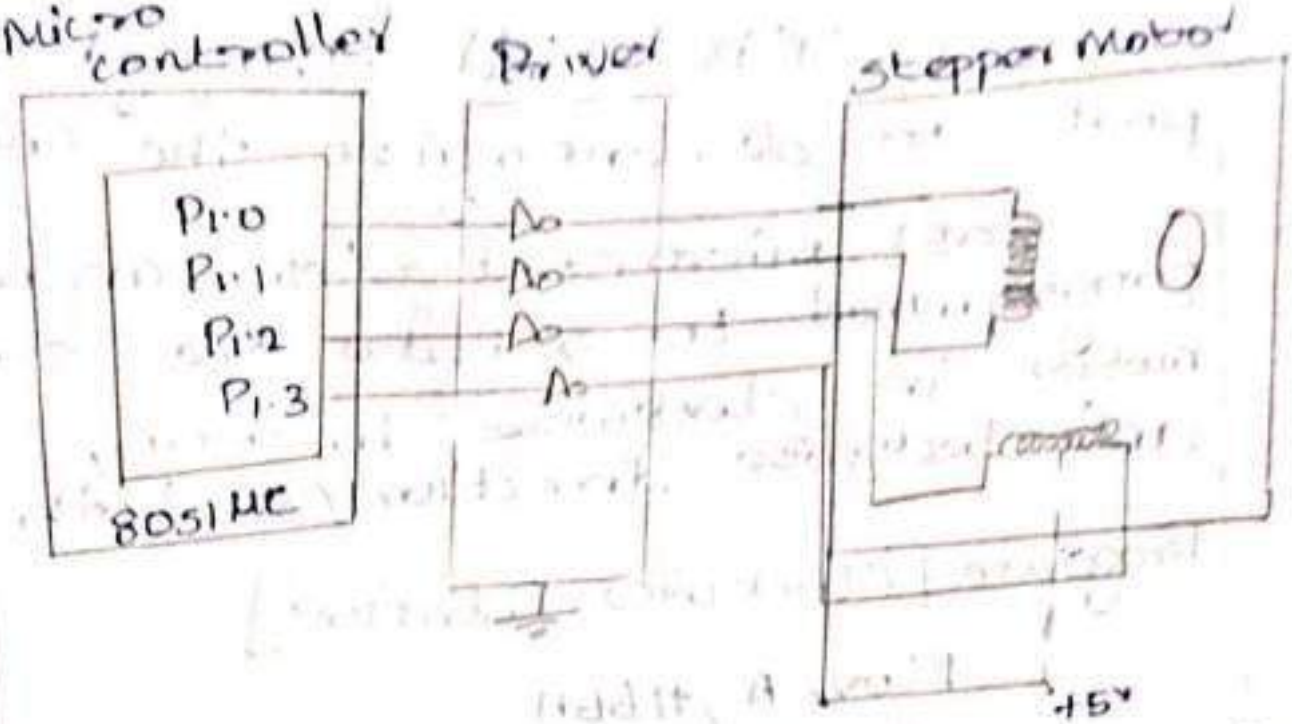
Stator winding

Step#	A	B	C	D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

Clock wise

Anti clock wise

Interfacing



The coils need to be energized for the rotation

This can be done by sending a bit sequence to one end of the coil

The bit sequence to one end of the coil

The micro controller 8051 has four IO ports P_0, P_1, P_2, P_3

Four pins from port 1 of 8051 normally $P_{1.0}, P_{1.1}, P_{1.2}, P_{1.3}$ are connected to the stator winding by the drives

We can program the micro controller 8051 by sending

electrical pulse to the one of the stator winding

Data '1' is send through the port to de-energize the coil.

8051 micro controller can be programmed to rotate the stepper motor in clockwise direction, anti clockwise direction (or) both.

Program [Clockwise Rotation]

```
      MOV A, #66H
      MOV P1, A
BACK: RRA
      ACALL DELAY
      SJMP BACK
DELAY: MOV R1, #100
UP1 : MOV R2, #50
UP2 : DJNZ R2, UP2
      DJNZ R1, UP1
      RET
```

Program [Anticlockwise Rotation]

```
      MOV A, #66H
      MOV P1, A
BACK: RLA
      ACALL DELAY
      SJMP BACK
```

```
DELAY: MOV R1, #100H
UP1  : MOV R2, #50H
UP2  : DJNZ R2, UP2
       DJNZ R1, UP1
       RET
```

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(Recognized Under Section 2(f) of UGC Act, 1956)
Permanent Affiliation for B.E. - Computer Science Engineering
Pottalkulam, Pothaiyadi Salai, Azhagappapuram Post, K.K.Dist. - 629 401.

Name P.S.Sree Vinisha Shalini Roll No 20RECO1 Branch ECE

Year / Semester III year/VI Semester Subject Code / Title EC8691- microprocessors and microcontrollers

Name of the Examination : Internal Exam I / II / III Total No. of Pages

Part-B

25/50 50

6) Architecture of 8086 microprocessor:

The 8086 CPU is divided into two parts namely

* Bus interface unit (BIU)
* Execution unit (EU)

* BIU and EU are function independently
* BIU are the most independent.
* EU receives the function software at BIU

BIU contains

* Segment Pointer
* instruction pointer
* instruction queue

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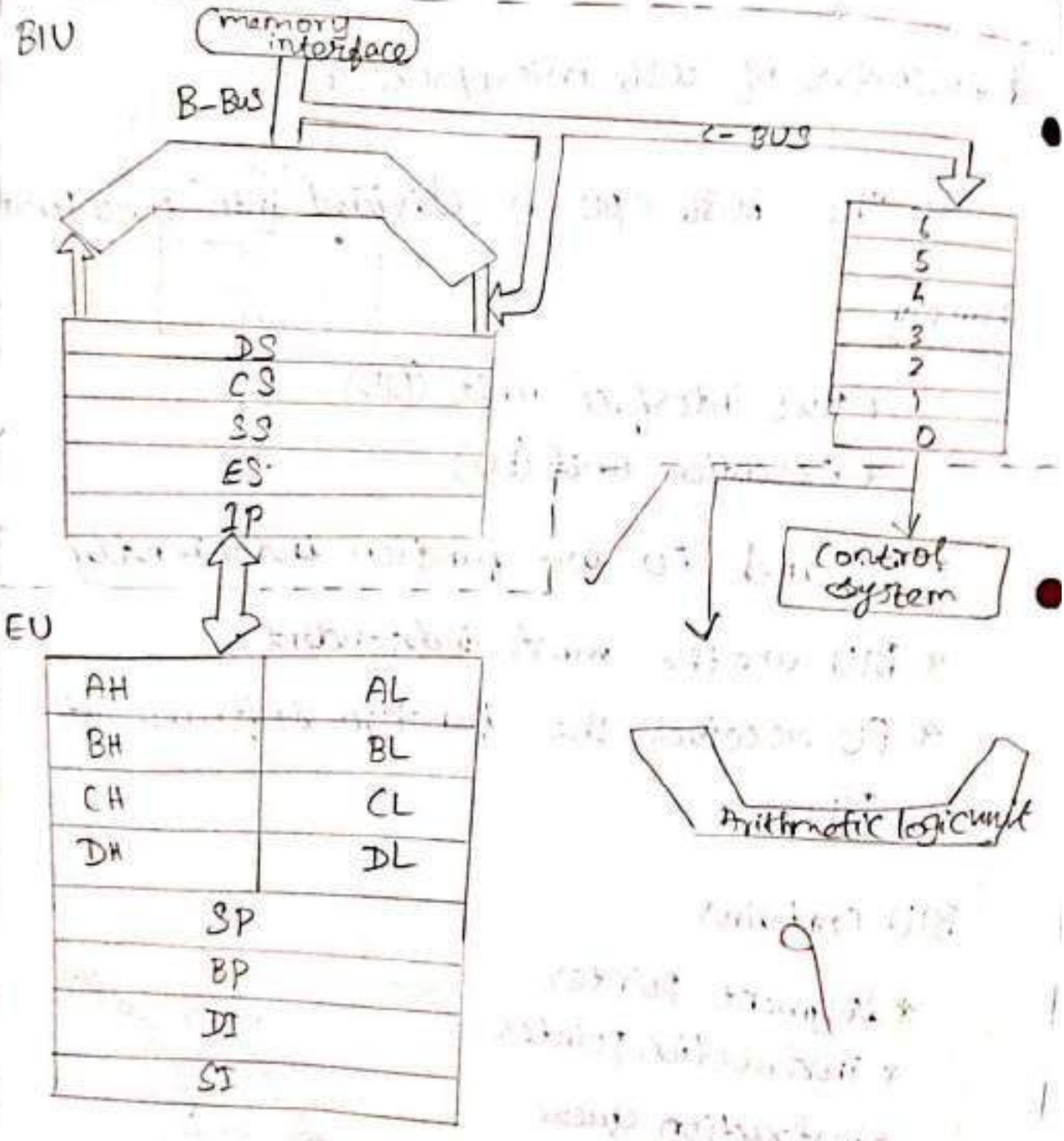
EU contains

* ALU
* General purpose registers
* ~~Stack~~ index
* Pointer



General purpose registers

General purpose register are used for same Purpose as ALU. It has 16 bit register.

Accumulator (AX)

* It has 16 bit registers and the two 8 bits are AL and AH.

* AL contains Lower order byte and AH contains higher order byte.

* AX is used for the instruction referenced by the program stack.

Base register (BX)

* It has 16 bit registers and the two 8bits are BL and BH

* BL contains Lower order byte of the word and BH contains higher order byte.

* Bx is used for the Base register and index register for the program stack.

Count register (CX)

* It is 16 bit register and two bit registers are CL and CH

* CL are contains Lower orderbyte and CH ase higher order byte.

* The CX is the instruction pointer to Counter the program data.

Data register (DX)

* It is 16 bit register and two bit registers are DL and DH

* DL contains Lower order byte and DH contains higher order byte.

* The DX is the used for the instruction Pointer to the program data.

Segment pointer:

Code Segment (CS)
Stack segment (SS)
Data segment (DS)
Extra segment (ES)

Code segment:

* It is a 16 bit register address containing 64 KB containing the procoded address.

* The program of an instruction referenced by the program instruction.

* Code segment cannot be allowed the program.

* code segment updated on FAR CALL, FAR RET respectively.

Stack segment:

* It is a 16 bit register address containing 64 KB containing the precoded address.

* The program of an data referenced by the program stack.

* Stack segment allow using POP instructions.

Data segment:

* It is a 16 bit register address containg 64 KB to preceded instruction.
* The program of an instruction referenced by the program data.
* The data segment can allocate using POP and LDS instruction.

Extra segment:

* It is a 16 bit register address Containing 64KB to precoded instruction.
* The program of an instruction referenced by the program data.
* The extra segment can allow using POP and LES instruction.

instruction pointer:

* It is 16 bit registers.

Pointer register

* stack pointer
* register pointer

Stack pointer:

It is a 16 bit register pointing to program stack.

Base pointer:

It is a 16 bit register pointing to the Base stack.

Index register

Source index: It is a 16 bit register and source data address.

destination index: It is 16 bit register and destination data address.

Flag register:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				OF	DF	IF	TF	SF	ZF		AF		PF		CF

Overflow flag (OF): It is set to the result is overflow.

Sign flag: It is set to the result is set.

Zero flag: It is set the result is zero.

Trap flag: It is set, Trap the result.

instruction queue.

* instruction queue is a first in first out (FIFO) instruction.

* The overlapping program fetch and execution.

ALU:

It is a 16 bit register, ALU fetches addition, subtraction, increament decreament etc...

7a) minimum mode of 8086:

* The minimum mode of 8086 is the describes the microprocessor of 8086 system, The ~~mic~~ 16 bit microprocessor of the minimum mode system.

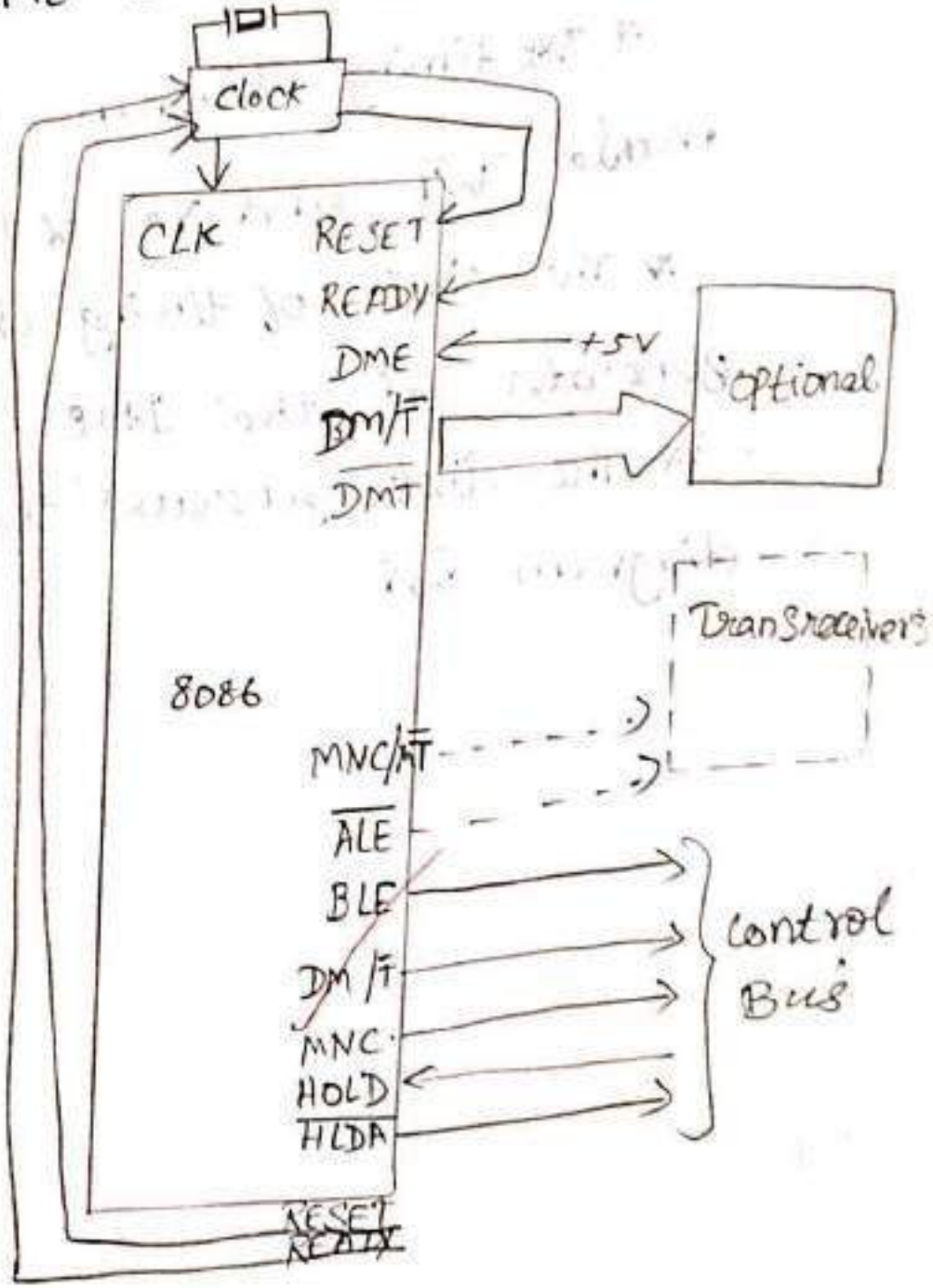
* The minimum mode system contains latches, memory, instruction counter and the microprocessor etc....

* The latches are the microprocessor system.

* The memory is the bidirectional Convinent of the instruction pointer of the system.

* There are two types namely: DME, DM/$\overline{T}$

* The DME is the differenent of the System



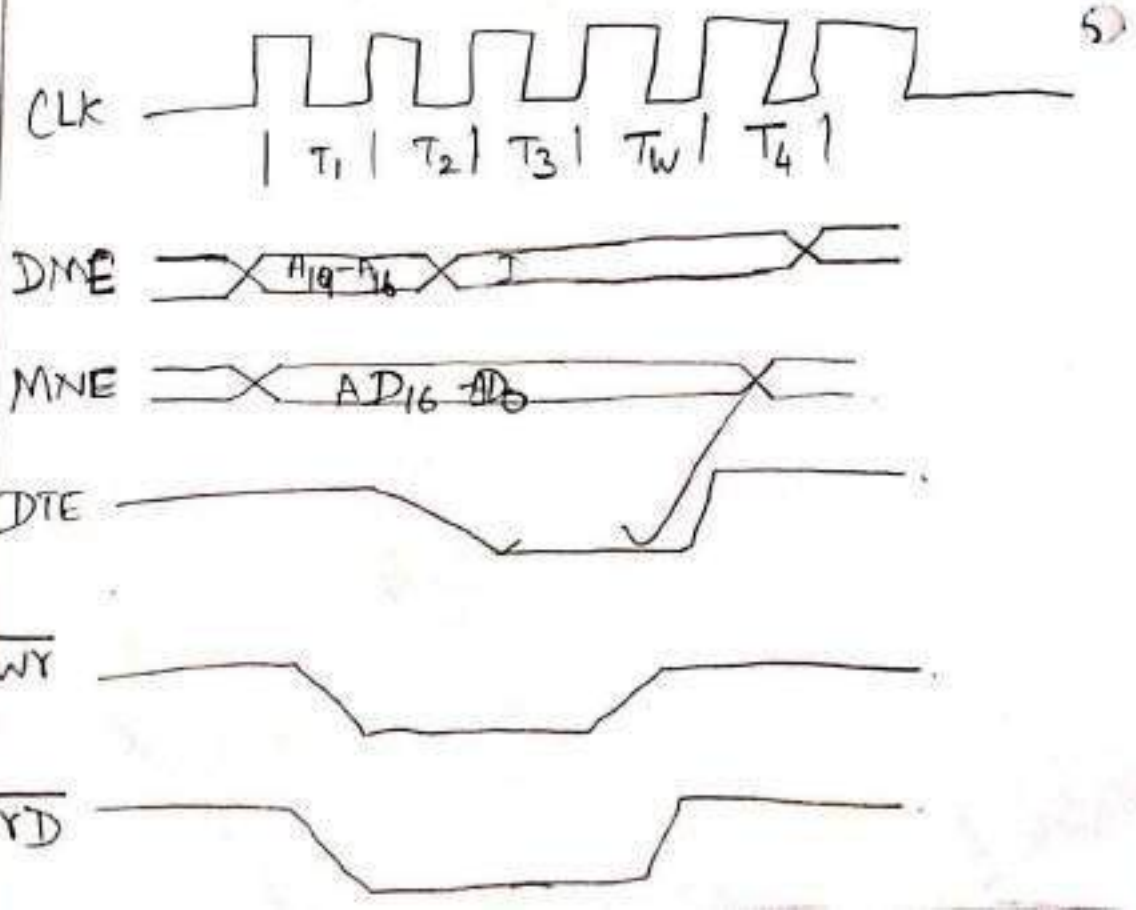
BUS Timing of the minimum mode:

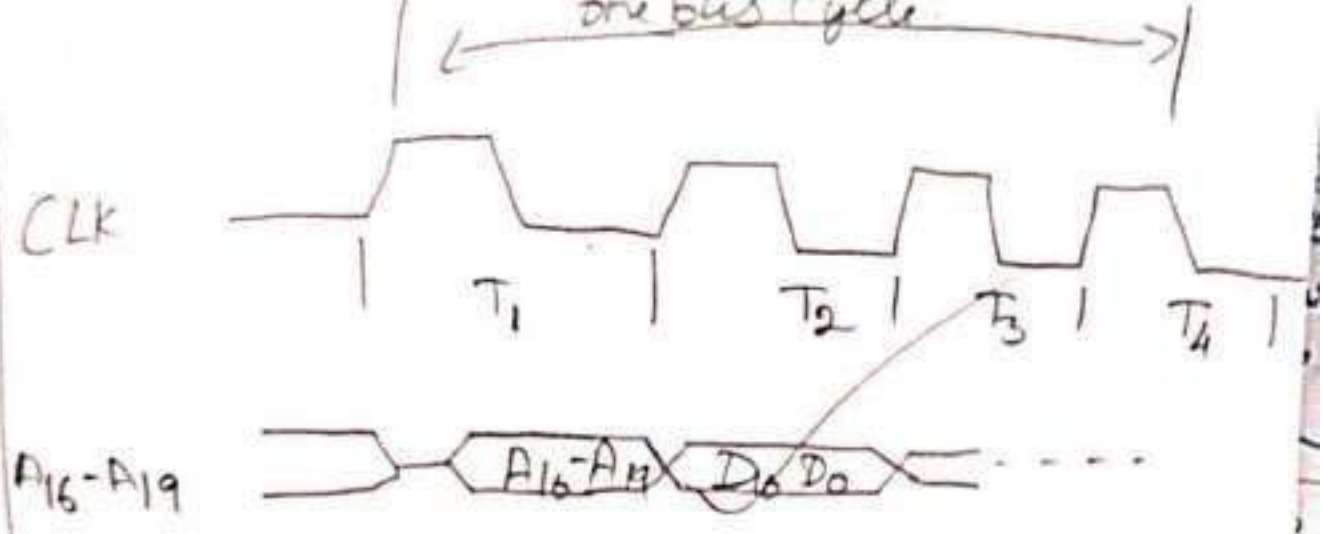
* The Bus timing of the minimum mode will generates at the two namely DMC DT/$\overline{R}$.

* The timing diagram of the minimum mode $\overline{WR}$ and $\overline{RD}$ of the Bus timing:

* The clock of timing diagram will generates at the DME.

* The clock generates the timing diagram $\overline{WR}$




one bus cycle
CLK
T1
T2
T3
T4
A16-A19
A16-A19
D0

A. Ahsan Akbar

III ECE

2016 ECO1

Class - test - 2

MPMC

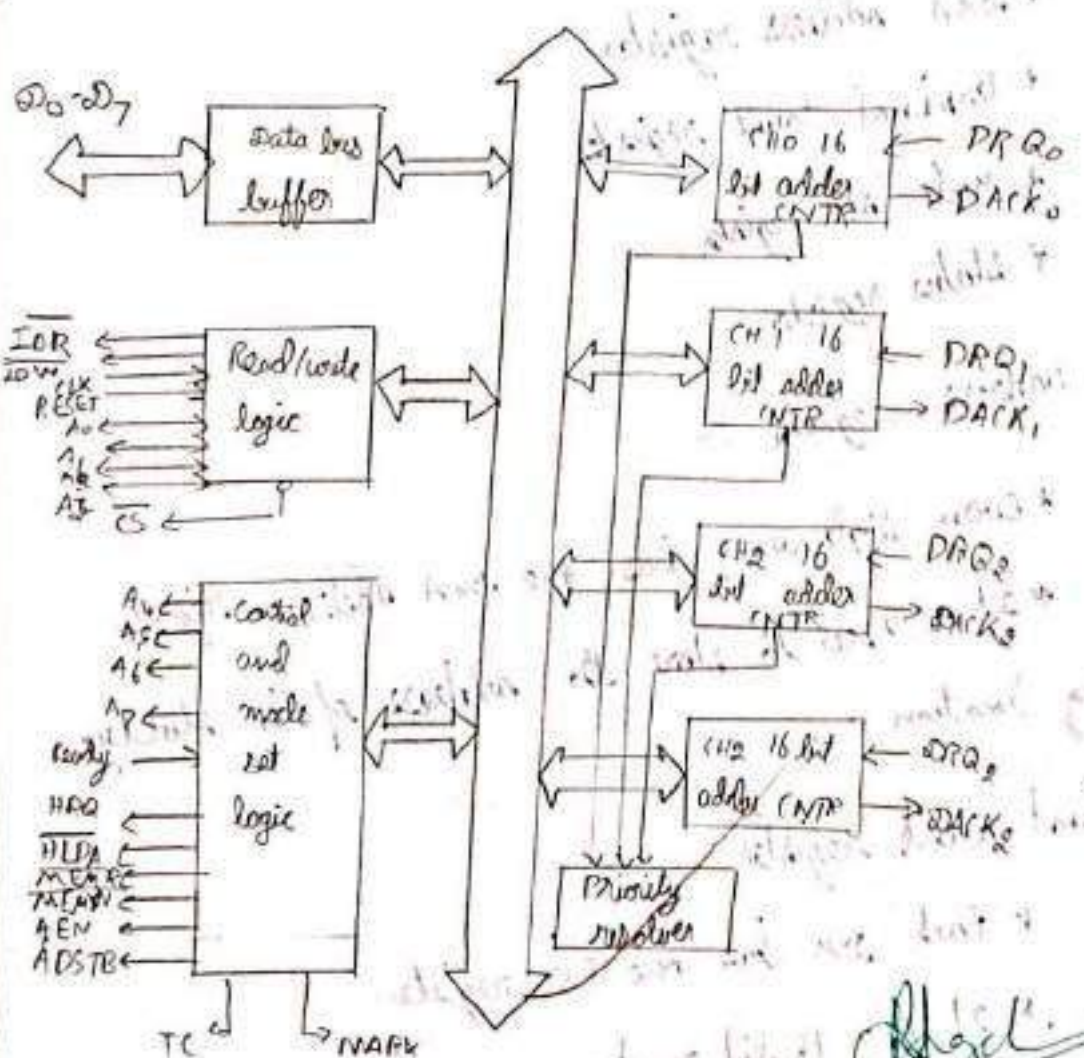
15/20

15-1-19

1. DMA :-

(i) Direct memory access is the fastest mode of transfer

(ii) In this mode the device will be transfer the data directly to the memory.



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* Intel 8257 is a four channel DMA controller.

* 8257 request the microprocessor for bus access using HOLD signal in minimum mode and RQ/GT signal in maximum mode

* 8257 handover the control of bus back to the CPU

Register of 8257:-

* DMA address register
* Terminal count register
* mode set register
* status register

DMA address register :-

* Every single DMA has one DMA address register
* It is used to store the address of the starting memory location.

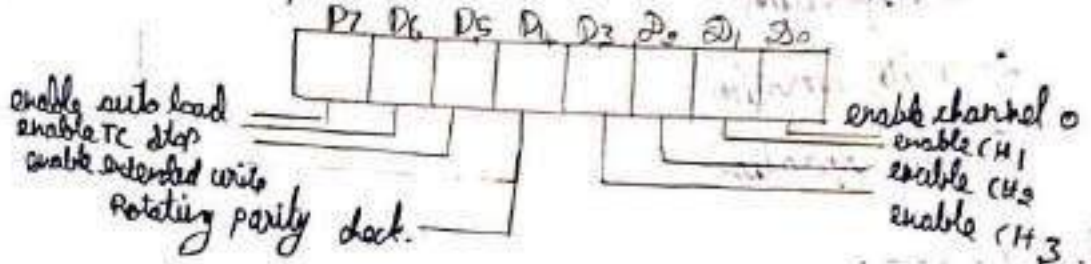
Terminal count register :-

* Each DMA has one TC register
* It is a 16 bit register.

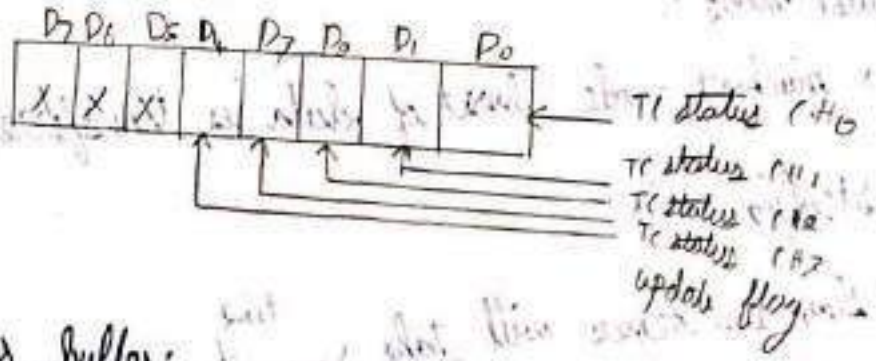
mode set register :

* It is used to program the 8257 as per the requirements of the system.

* If TC stop bit = 1, selected channel is disabled.
* If auto load bit = 1, it enables channel 2 for the repeat block operation



Status register :



Data bus buffer :

* 8 bit tri state bidirectional buffer. It interfaces the internal bus of 8257 with external system bus.

Read / write logic :

* In slave mode, it accepts I/O read or I/O write signal
* In master mode, it generates $\overline{IOW}$ or $\overline{IOR}$

Control unit :-

It generates required control signals like $\overline{IOR}$, $\overline{IOSTB}$, $\overline{MEMR}$, $\overline{MEMW}$, TC etc...

Priority register :-

It resolves the priority of four DMA channels.

DMA transfer and operation :-

1. DMA operation
2. Write operation
3. Read operation

Modes of 8257 :-

1. Burst mode :-

* Quickest mode, burst of data is transferred by 8257

2. Cycle stealing mode :-

* Slow I/O devices will take some time to prepare data
* CPU keeps control of buses.

3. Interleaving mode :-

* Whenever CPU does not require the system buses, then only control of buses will be given to DMAC.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

INTERNAL TEST-I

Subject Code/ Subject Name:EC8691 Microprocessors and Microcontrollers

Time: 2.00-3.30 PM

Year/Branch : III ECE

Date: 15/3/2023

Part: A(5*2=10)

Q.No	COs	Cognitive Level	Questions
1	CO1	K1	Draw the format of 8086 flag register
2	CO1	K1	What is linker?
3	CO1	K1	Calculate the physical address, when segment address is 1085H and effective address is 45371L.
4	CO2	K2	What is the operation of S0, S1 and S2 pins in maximum mode?
5	CO2	K4	In an 8086 microprocessor, the contents of the accumulator and the carry flag are A7 (in hex) and 0, respectively. If the instruction RLC is executed, then the contents of the accumulator (in hex) and the carry flag, respectively, will be-------- (GATE-2016)

Part: B(2*16=32)

Q.No	COs	Cognitive Level	Questions
6(a)	CO1	K3	Explain the data transfer group and logical group of 8086 instructions
			OR
6(b)	CO1	K2	Explain the internal hardware architecture of 8086 microprocessor with neat diagram
7(a)	CO2	K3	Draw and explain the minimum mode of 8086
			OR
7(b)	CO2	K3	Explain closely coupled and loosely coupled configuration

Part: C(1*8=8)

Q.No	COs	Cognitive Level	Questions
8 (a)	CO1	K3	Explain different types of interrupts in 8086
			OR
8 (b)	CO2	K3	Write about coprocessor configuration

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AVK Nagar,, Pottalkualm, AzhagappapuramP.O.kanyakumari District–629 401

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

INTERNAL TEST-II

Subject Code/ Subject Name: EC8691 Microprocessors and Microcontrollers

Time: 11.00-12.30 PM

Year/Branch : III ECE

Date: 18/3/2023

Part: A(5*2=10)

Q.No	COs	Cognitive Level	Questions
1	CO3	K1	Mention the features of 8251 Serial Communication Interface
2	CO3	K1	Differentiate memory mapped I/O and I/O mapped I/O
3	CO4	K1	Write an ALP in 8051 to multiply the given number 55h and 87h. [Gate 2016]
4	CO4	K2	Write about BIT manipulation instructions of 8051.
5	CO4	K4	Write a program to add two 16 bit nos in 8051. The numbers are 4590 and 1234 . Store the sum in R7 and R6.

Part: B(2*16=32)

Q.No	COs	Cognitive Level	Questions
6(a)	CO3	K3	Explain in detail about serial communication interface-8251 with neat block diagram
			OR
6(b)	CO3	K3	Draw the functional block diagram of 8254 programmable interval timer and explain the different modes of operation.
7(a)	CO4	K3	With neat diagram explain the architecture of 8051 microcontroller
			OR
7(b)	CO4	K3	(i) Memory organization of 8051 (ii) Port P0 and P1 circuits

Part: C(1*8=8)

Q.No	COs	Cognitive Level	Questions
8 (a)	CO3	K3	Describe Traffic light controller interfacing .also write the program code.
			OR
8 (b)	CO4	K3	Illustrate the different addressing modes of 8051

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Name V. Gianga Roll No. : 20RE102 Branch : ECE
Year / Semester III year Subject Code / Title EC2691 Microprocessors and microcontroller
Name of the Examination : Internal Exam I / II / III Total No. of Pages

Part - B 42/50 84%

6(b). Architecture of 8086 :-

The 8086 cpu is divided into two independent functional ports.

1. Bus interface unit (BIU)
2. Execution unit (EU)

* The BIU interface the 8086 to the outside world. The BIU fetches read data from memory and ports. and write data to memory and I/O ports.

* EU receives the program instruction code and memory from the BIU, executes these instructions and the results stored the general registers and the output put all the data through the BIU.

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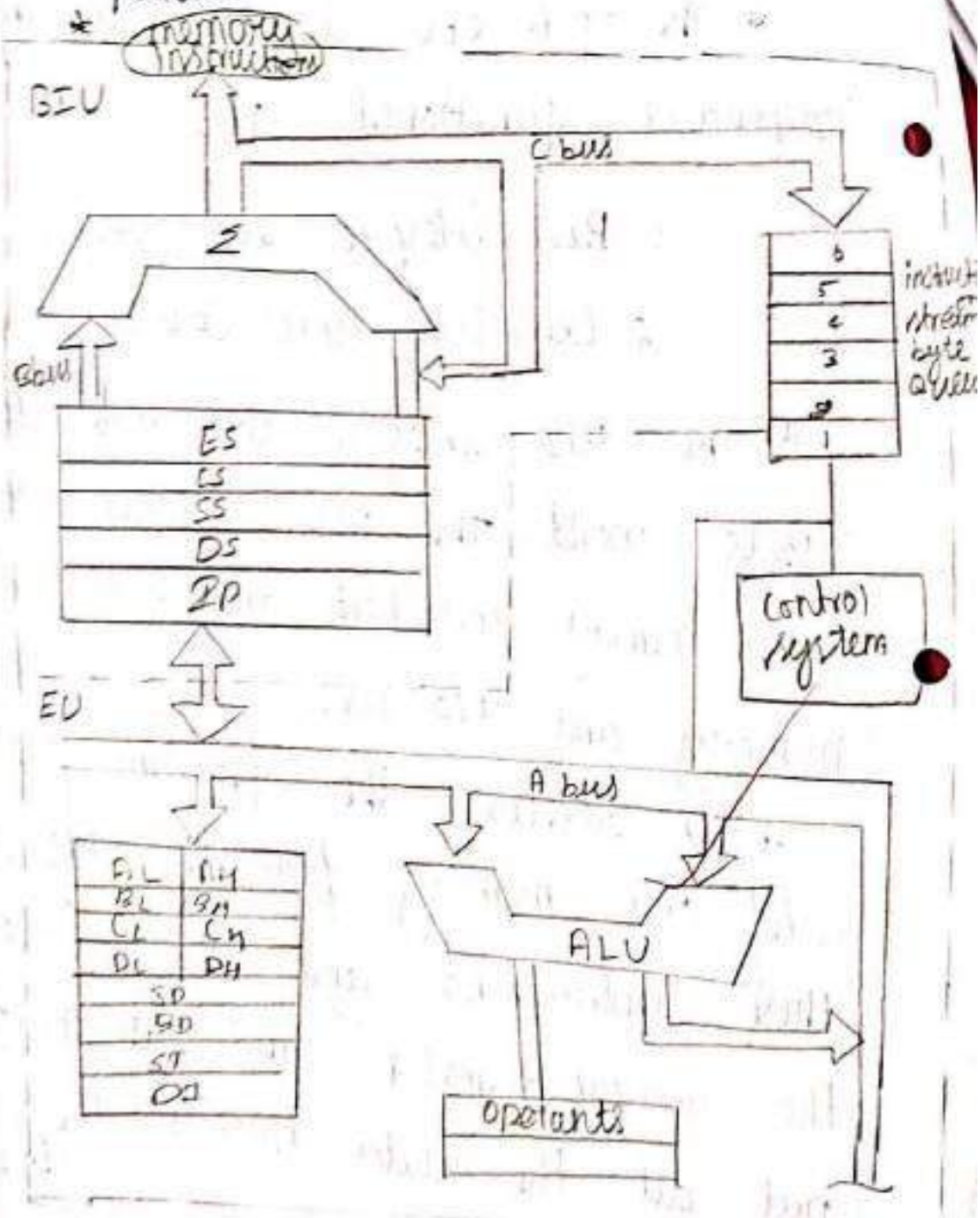
BIU contain -

* segment register
* instruction pointer
* instruction Queue

EU contain -

* ALU
* general purpose registers
* Index registers
* pointers
*



General Registers :-

* The general purpose registers are,
  1. Accumulater register (AX)
  2. Base register (BX)
  3. Count register (CX)
  4. Data register (DX).

1. Accumulater Register (AX) :-

* Accumulater register is the 16 bit register also divided into two 8 bit registers AL and AH.
* AL contain Lower order byte and AH contain higher order byte.
* Accumulater can be used for I/O operation and string manipulation.

2. Base Register (BX) :-

* Base register is a 16 bit register also contain two 8 bit registers BL and BH.
* BL contain lower order byte and BH contain higher order byte.
* BL can contain a data byte used for Based, Based indexed and register indirect addressing.

3. count register (CX):-

* count register is a 16 bit register contain two 8-bit registers CL and CH
* CL contain lower order byte and CH contain higher order byte.
* CL can contain string manipulation and shift/rotate registers.

4. Data register (DX):-

* Data register is a 16 bit register also contain two 8 bit registers dL and DH.
* DL contain lower order bytes DH contain higher order byte.
* DL can be used as an numbers in the I/o operation.

Segment Registers:-

* The segment registers are,
  1. code segment (CS)
  2. Stack segment (SS)
  3. data segment (DS)
  4. extra segment (ES)

1. Code segment :-

* Code segment is a 16 bit register contain address 64 KB segment with processor instruction.

* Code segment cannot be changed directly.

2. Stack segment :-

* Stack segment is a 16 bit register contain address 64 KB segment with program Stack.

* By default the processor assume that the all data instructions referenced by Stack pointer and Base pointer registers located at the Stack segment.

* Stack segment can be changed directly using pop instructions.

3. Data segment :-

* Data segment is a 16 bit register contain address 64 KB segment with program data.

By default the processor assume that the all data referenced by general registers and index registers located at

the data segment.

* data segment can be change directly using pop and LDS instru

4. Extra segment:-

* Extra segment is a 16 bit register.

* ES can be changed directly using pop and LES instructions.

Pointers:-

Stack pointer:-

* Stack pointer is a 16 bit register pointing to program Stack

Base pointer:-

* Bp is a 16 bit register pointing to data the program stack

Index registers:-

Source indexed (SI):-

* SI is a 16 bit register

* SI is used for based, based indexed as well as source data address string manipulation.

destination indexed (DI):-

* DI is a 16 bit register
* It is used for based, based indexed as well as destination data address string manipulation.

Instruction pointer (IP):-

* IP is the 16 bit register.
* The operation same as the program counter.

Flags:-

* Flags is the 16 bit register also contain nine 1 bit flags

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				OF	DF	IF	TF	SF	ZF		AF		PF		CF

Conditional flags:- OF, SF, ZF, PF, AF, CF

Control flags:- DF, IF, TF

OF :- Coverflow flag :-) :-

* It is set if the overflow occurs

SF :- Sign Flag:

* It is set if the most significant bit of the result is set.

Zero flag :-

* If the set there is no re...

Trap flag :-

* If the set, the trap execute...

after every instruction

Instruction Queue :-

* The Instruction Queue is the first In first Out [FIFO) group of registers. where the 6 bits instruction code is from memory.

Arithmetic and logic unit :-

* It is a 16 bit register. It can add, subtract, increment, decrement and perform AND, OR, NOT, XOR

11(a) Minimum mode configuration:-

* Minimum mode pin 33 - MN/MX = 1.
* All the control signals are given out the microprocessor chip itself
* There is only single microprocessor in the minimum mode configuration
* The remain components are, latches, Tranceivers, clock generator, memory, I/O devices.
* Latches are generally a D Flip Flop like IC 8282.
* They are used for separation of valid address from multiplexed Address data signal.
* Latches are controlled by ALE.
* Three latches are used for 20 Address lines.
* Transceivers act a bidirectional buffers.

* Transceivers are used for separate data from the time multiplexed address data signals.

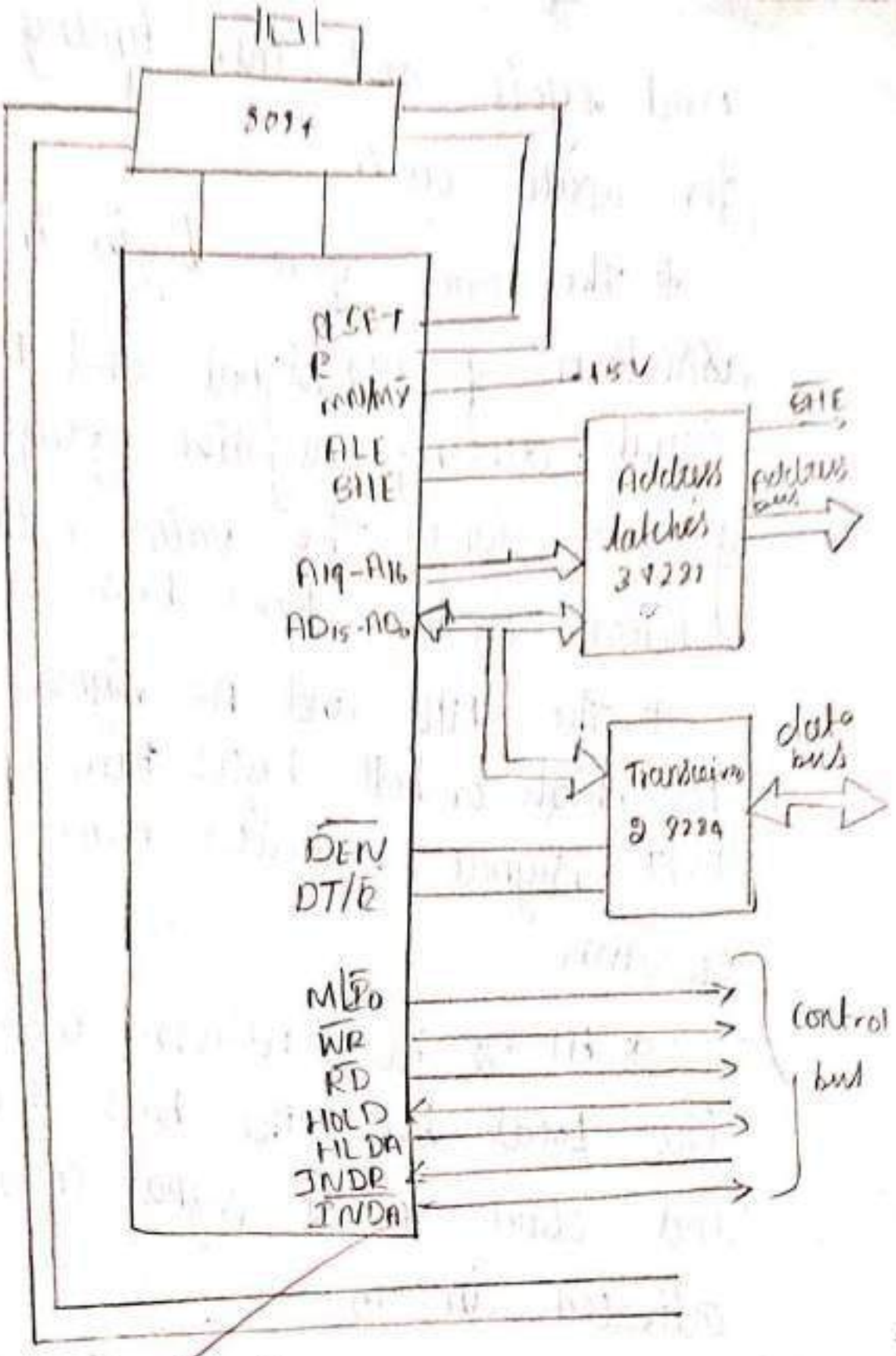
* they are controlled by DEN and DT/$\overline{R}$.

* Memory contain monitor & user program storage.

* EEprom used for monitor storage

* RAM used for user program storage.

* clock generator are generates the clock from the crystal oscillator. Then shape it and make to it's more precisious. they are used for accurate timing referenced in the minimum mode.



Bus timing for minimum mode :-

* The opcode fetch and Read cycle are similar. Hence the timing diagram can be catorgrized into two parts. The first part is timing diagram for

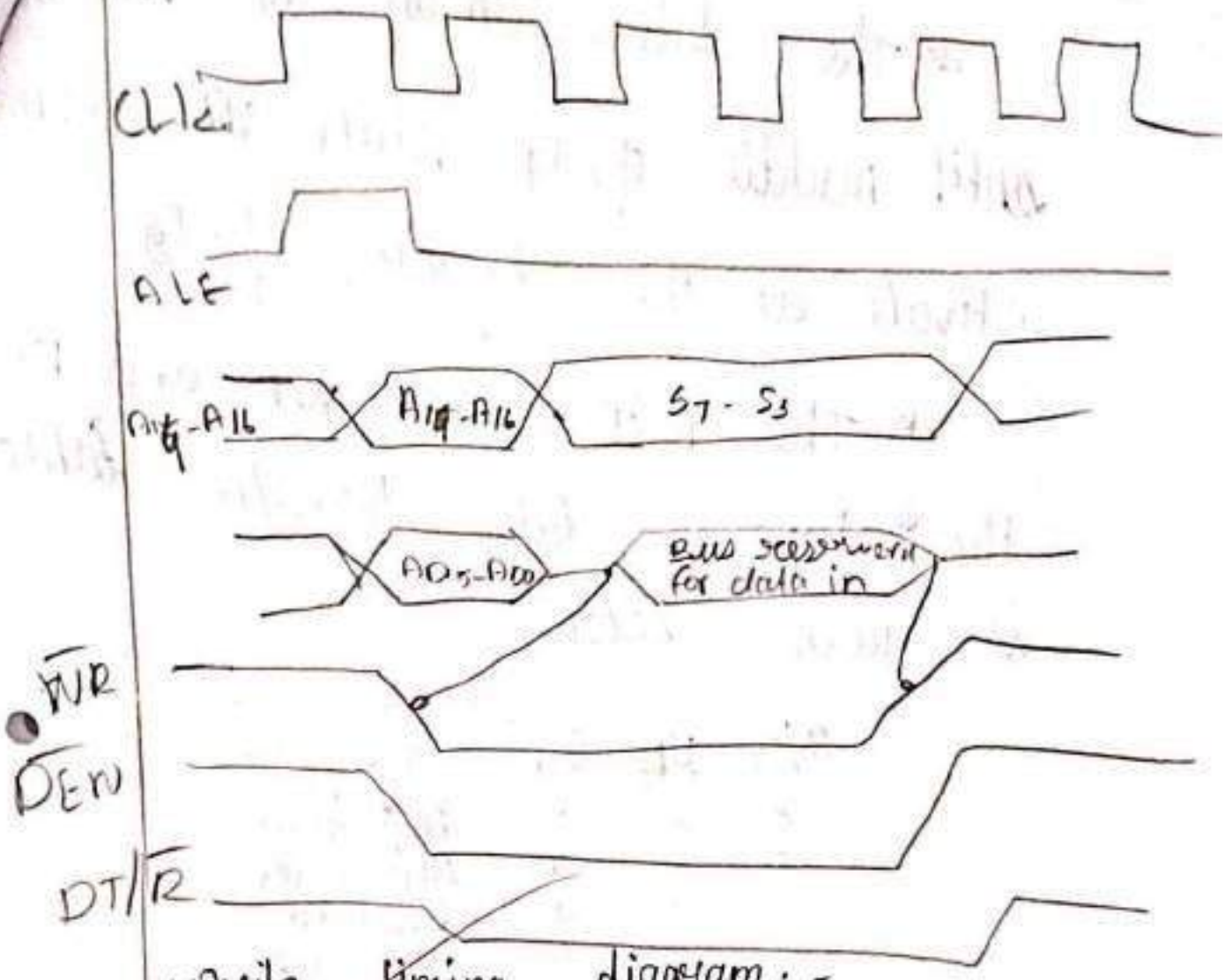
Read cycle and other timing di... for write cycle.

* The read cycle begin in T_1 wi... assertion of (ALE) signal and M/IO signal. during negative going edge of this signal. The valid address latched on the local bus.

* The BHE and A_0 signals address low, high or both bytes. From T_1 to T_4 the M/IO signal indicates memory or I/O operation.

* AT T_2, the Address removed from the Local bus, the bus then tristated and read control signal (RD) also activated in T_2.

* The Read signal causes the Addressed device to enable its data bus drivers. At RD goes low the valid data is available on the data bus.



write timing diagram :-

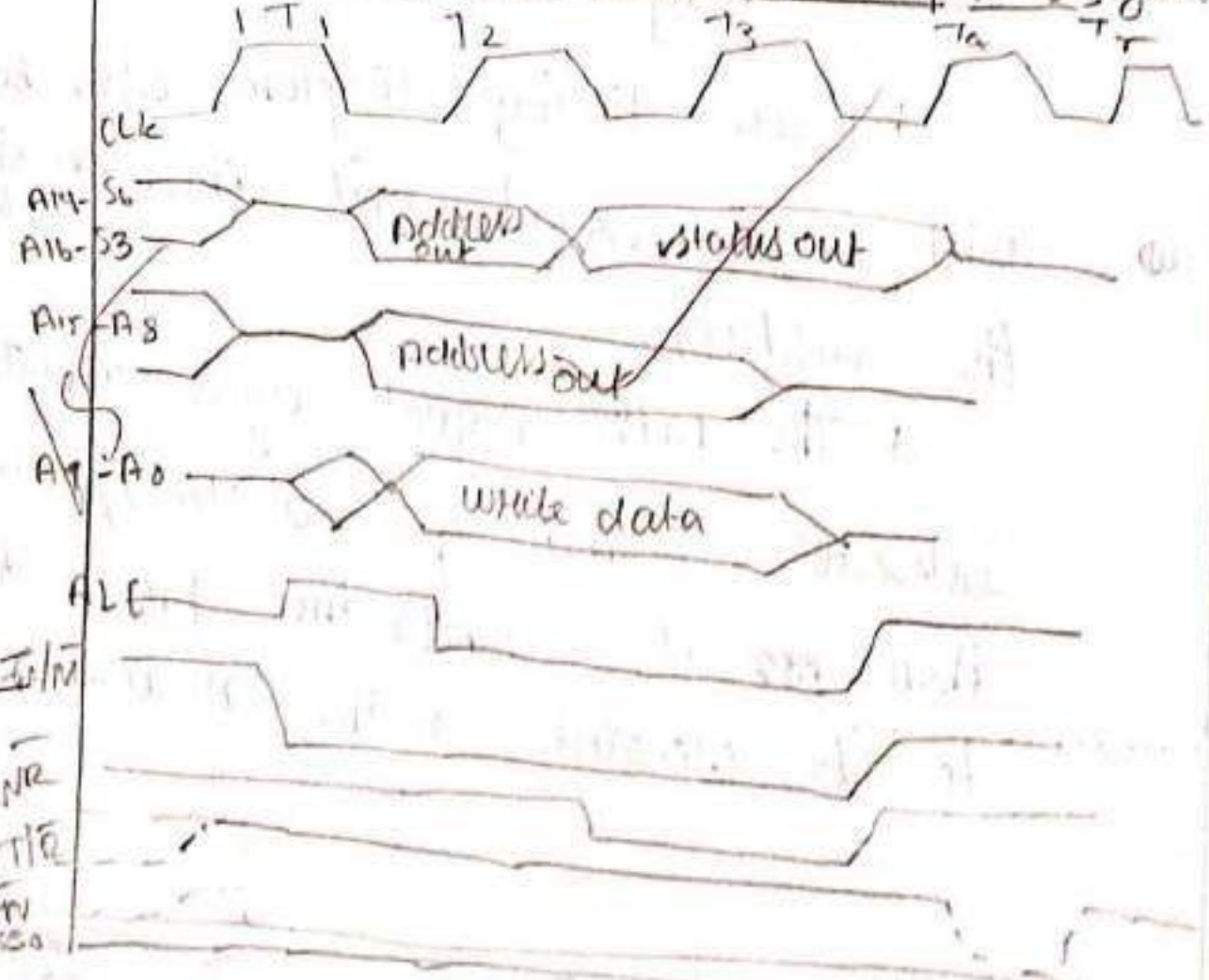
* write timing diagram also begi. with ALE signal and Emission of the address.

* The M/IO signal again asserted indicates a memory and I/O operation then it sends the process data to be located on the Address

* The data remain on the until middle of T4 state WR become activate at the begining of T3.

* The M/IO and WR and RD the type of data transfer table is given below.

M/IO	RD	WR	Transfer type
0	0	1	IO read
0	1	0	IO write
1	0	1	Read data
1	1	0	write data.



Part : c.

8(b) Co processor configuration :-

* The co processor and closely coupled configuration are similar to both the CPU and the external processor.

shares :-

* memory
* I/o system
* clock generator
* Bus and Bus control logic.

* WAIT instruction allows the processor to synchronized itself.

* TEST input is asserted (low) wait state is completed and executes next instruction.

* ESC instruction :- ESC opcode, operand.

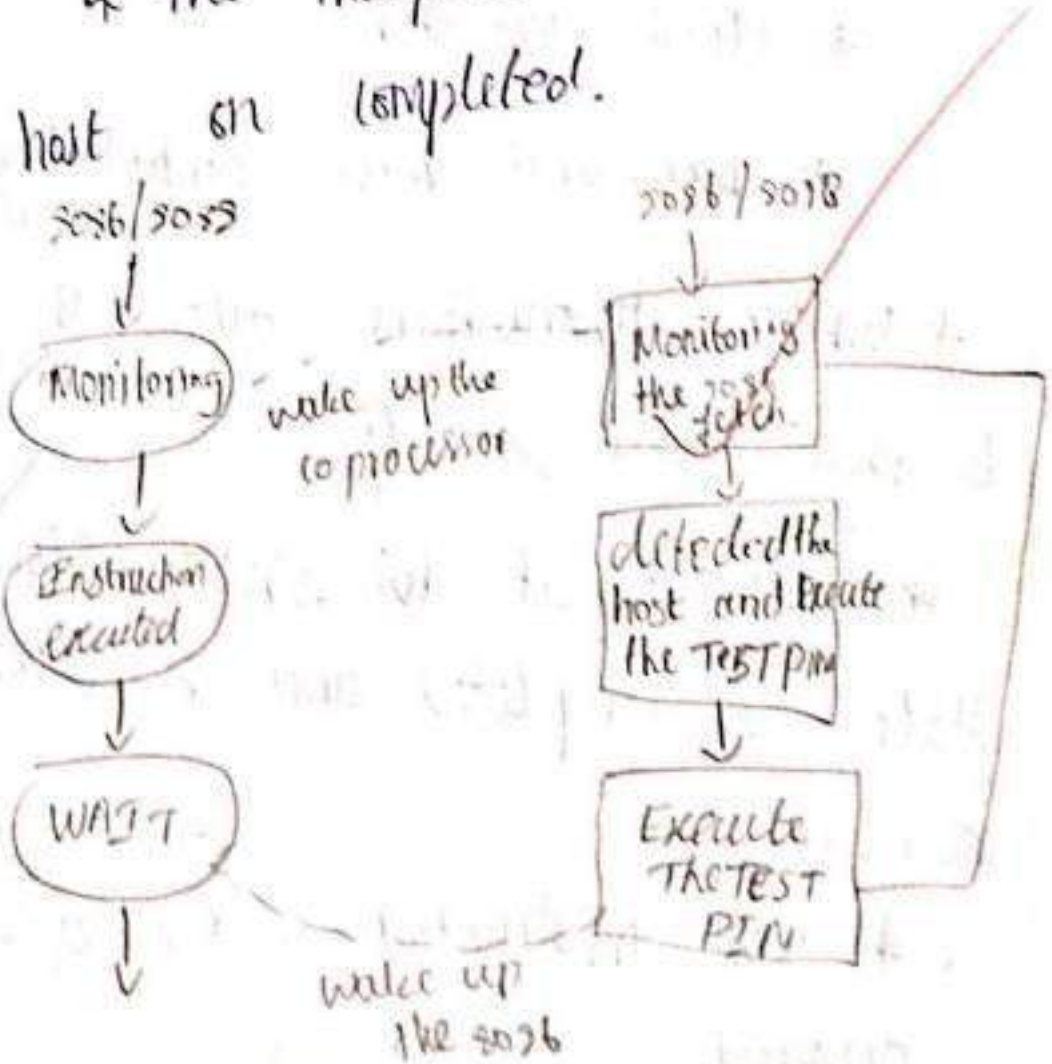
* The coprocessor cannot take of the control signals it does everything through the CPU.

* the 8086 shares CPU and clock and bus control logic

* The communication with the host CPU by the way of shared.

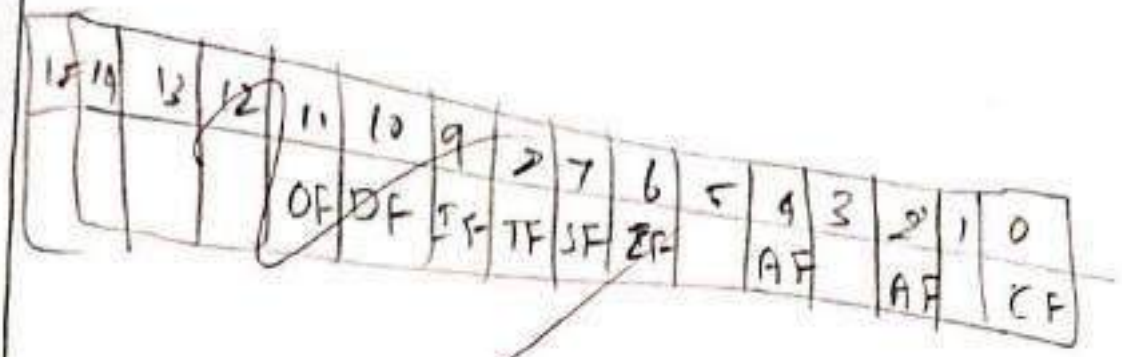
* The host set up the message in monitor.

* the independent host interrupt host on completed.



Pool : A

1.



2.

3. Physical address = segment address x 10H + effective address.

= 1085H x 10H + 4537H

= 10850 + 4537H

Physical address = 15387H.
(20bits).

5. Content of the accumulator and the carry flag will be 4 and 1.

Assignment - 1

Micro Processor And Micro Controller

Assembler Directives of 8086

10

Submitted by,
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Assembler Directives

An assembler is a program used to convert an assembly language program into the equivalent machine code modules which may further converted into executable codes.

Some directives such as ORG, EQU, DB, DW, etc which are common in different assembler were also described. Though a representative set of directives on the for the 8086 assembler is presented it is possible that some assembler have a few additional directives. On the other hand some of the directives presented here may not be present or may be present in different forms.

Directives for constant and variable Definition.

An Intel 8086 assembly program uses different types of constants like binary, decimal, octal and hexadecimal. These can be represented in the program using different suffixes like B, for binary decimal D (for octal) and H (for hexadecimal) to the constant

10H is a hexadecimal number

27O is an octal number.

10100B is a binary number.

A number of directives are used to define and store different kinds of constants

The Define byte, Define word, Define Doub word.

The 8086 assembler uses DD as directive to double word.

* DQ : define Quad word
* DT : Define Ten bytes.

DUP

using the DUP directive, several locations ma be initialized and the values may be put in the locations The formate is as follows. Name Type Num

Example: TEMP DB 20 DUP(5)

The directive define an array of 20 bytes memory and each location is initialized to 5 The array is named TEMP.

EQU

The EQU directive may be used to define a data name with immediate value or another data name. It can also even be used to equate a name to a string.

Example: NUMB EQU 20H

NAME EQU "RASHMI"

Program location control Directives.

The directives used for program location control in the 8086 assembler are (ORG, EVEN, ALIGN and LABEL).

ORG

The ORG directive is used to set the location counter to a particular value.

Ex: ORG 2375H

The location counter is set to 2375 H. If it occurs in data segment the next data storage will start at 2375H. If it is in code segment the next instruction will start at 2375H

EVEN

Using EVEN directive, the next data item label is made to start at the even address boundary. The assembler on encountering EVEN directive will advance the location counter to even address boundary

* EVEN TABLE DW 20 DUP(0)

This statement declares an array named TABLE of 20 words starting for the even address

ALIGN number

This directive will force the assembler to align the next segment to an address that is divisible by 2, 4, 8 or 16. The unused bytes are

* ALIGN 2

It will force the next segment to the next even address.

LENGTH

It is an operator which is used to tell the assembler to determine the number of elements in a data item, such as string or array.

MOV AX , OFFSET FACT

This statement will place in the AX register the offset of the variable FACT from the start of the segment.

OFFSET

This operator is used to determine through the assembler the offset of a data item from the start of the segment containing.

Example : MOV AX , OFFSET FACT

This statement will place in AX register the offset of the variable FACT from the start of the segment

LABEL.

The LABEL directive is used to assign a name to the current value in the location counter. The location counter denoted is used by the assembler to keep track of the current location. The value in the location counter denotes the distance of the current location

Segment Declaration Directives.

These directives help in declaring various segments with specific names. The start and the end of segments may also specified using this directive. The directives for segment declaration include SEGMENT, ENDS, ASSUME, GROUP, CODE, DATA, STACK are

SEGMENT and ENDS.

The SEGMENT and ENDS directives signify the start and end of a segment

INST SEGMENT.

ASSUME CS : INST, DS : DATA W.

INST ENDS ASSUME

The directive is used to assign logical segment to physical segment at any time.

Example : ASSUME : CODE, DS : DATA / SS : STACK

This directive tells the assembler that the CS register will store the address of the segment whose name is CODE and so on

.CODE (Name).

This code directive is the short cut used in the definition of code segments. The name is optional and is specified if there is more than one code segment in the program.

.DATA and .STACK.

Similar to .CODE the .DATA and .STACK directives are short cuts in the definition of data segment and stack segment, respectively.

GROUP.

This device is used to tell the assembler to group all the segments in one logical group segment. This allows the contents of all the segments to be accessed from the same segment base.

Eg: PROG GROUP CODE, DATA

The above statement will groups the two segment CODE and DATA into one segment named PROG. Each segment must be declared using ASSUME statement

ASSUME CS : PROG DS : PROG

Procedure and Macro-related Directives.

The directives in this group relate to the declaration of procedures and macros along with the variables contained in them. The directives include PROC, ENDP, PUBLIC, MACRO, ENDM and EXTRN

PROC and ENDP.

The PROC directive is used to define the Procedures. The procedure name is a must and it must follow the naming convention of the assembler

The ENDP directive is used to mark the end of the procedure. Some examples

```
FUNCT PROC FAR
  ——
  ——

  ENDP
FACT PROC NEAR
  ——
  ——
ENDP
```

The first procedure FUNCT is in a segment which is different from where it is called. The

word procedure. FACT is in the same segment where it is called. All the statement of the procedure are between PROC and ENDP directives.

PUBLIC.

It is very much possible that a variables is defined in one module but is used in other modules In order to facilitate the linking, such variables are declared public, using the PUBLIC directive in the module.

PUBLIC PX, PY, PZ.

MACRO and ENDM

The MACRO directive is used to define macros in the program. The ENDM directive defines the end of MACRO

Other Directives

These directives are of general nature, or they relate to more than one group described earlier. The PTR, PAGE, TITLE, NAME and END

PTR.

The PTR is an operator used in instructions to assign a specific type to a variable or a label. The PTR operator can also be used to override the

declared type of variable.

ARRAY DW 0125H, 1630H, 9215H ...

In the above array of words, suppose we wish to move a byte from the array, we may then simply insert the PTR operator.

MOV AL, BYTE PTR ARRAY.

PAGE:

The directive is used for listing of the assembled program. At the start of the program the directive is placed to specify the maximum number of lines on a page and the maximum number of characters

PAGE 60, 120.

The above example specifies that 60 lines are to be listed on a page with a maximum of 120 characters in each line.

TITLE

This directive is also used for the listing of the program. The title declared in this directive defines the title of the program and is listed in the s of each page of program listing.

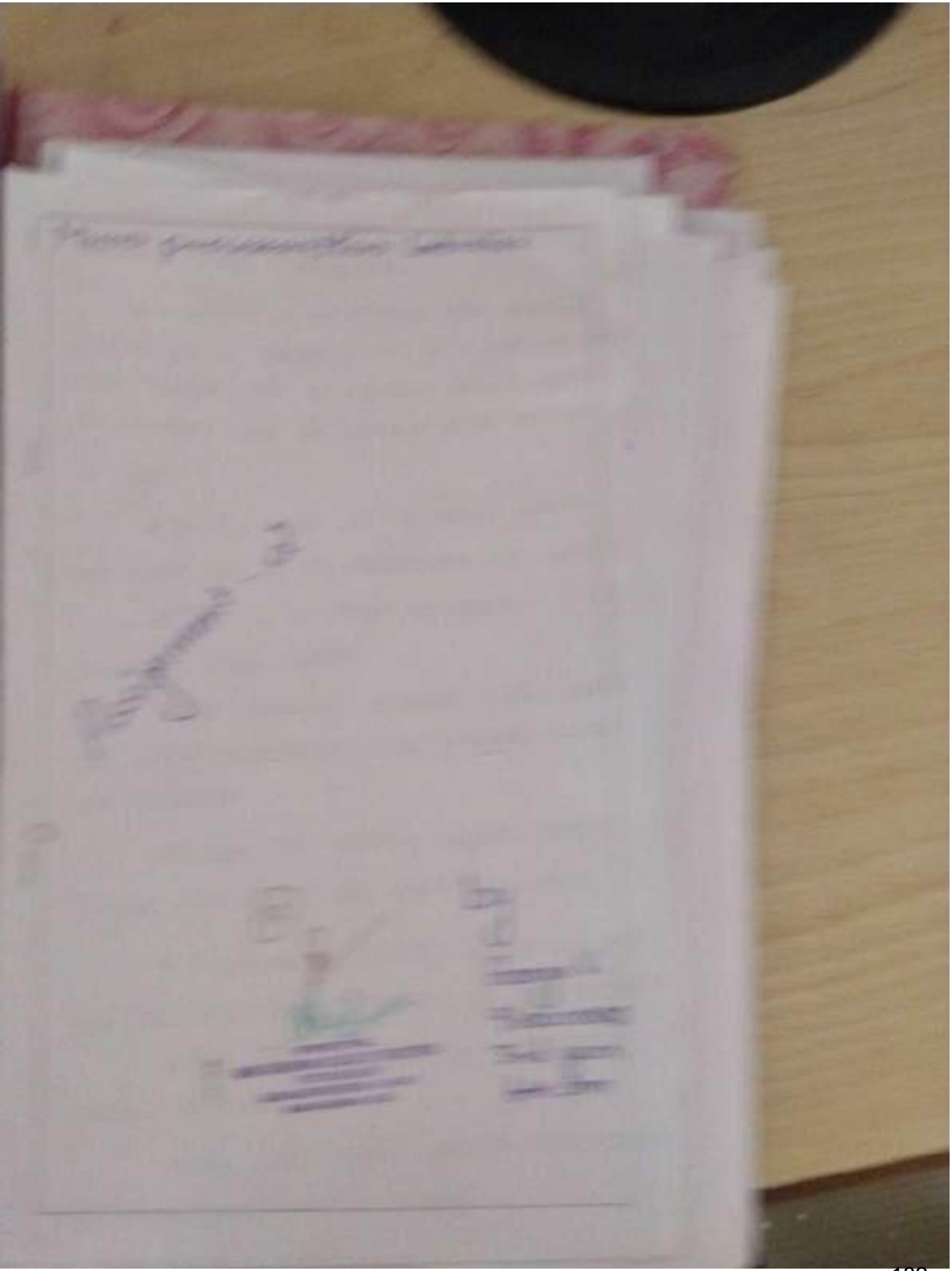
Eg. TITLE PROGRAM TO FIND SQUARE ROOT

NAME

The NAME directive is used to assign a specific name to each module, when the program consists of a number of modules. This helps in understanding the program logic.

END.

This is the last statement of the program and it specifies the end of the program user assembler. It must be noted that not all of the above directives are used in all program. User may deploy them depending on the need of the program logic.



Micro processors & Micro Controller

Assignment - 2

(10)

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6th Sem

Minimum Mode Configuration :-

* A processor is an minimum mode when its MN/MX pin is strapped to +5V. In a minimum m 8086 system, the microprocessor 8086 is operated in minimum mode by strapping its MN/MX pin to logic 1.

* In this mode, all the control signals are given out by the microprocessor chip itself.

* There is a single microprocessor in the minimum mode system.

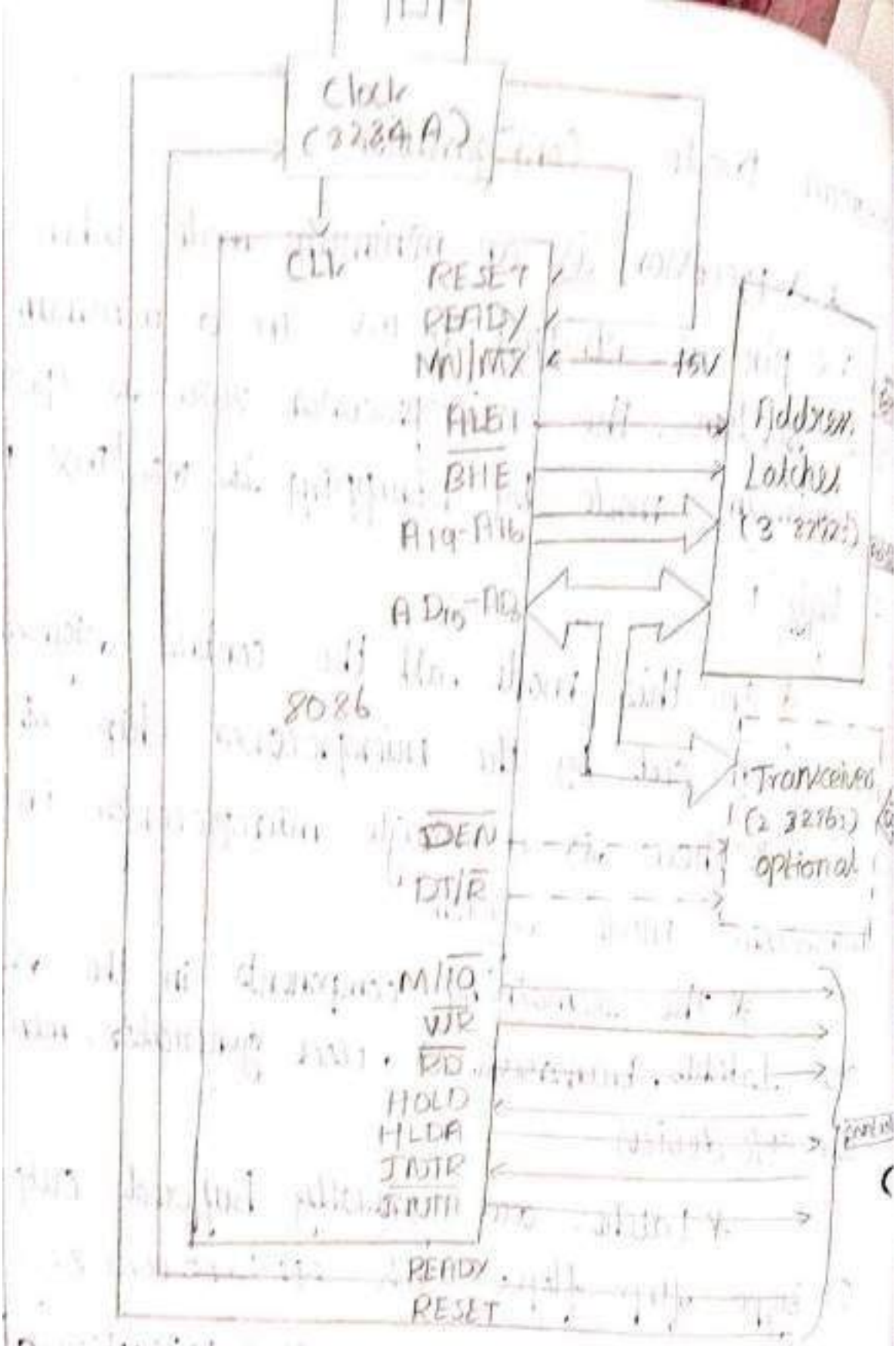
* The remaining components in the system are latches, transreceivers, clock generator, memory and I/o devices.

* Latches are generally buffered output D-type flip flops like 74LS373 (or) 8282.

* Transreceivers are the bidirectional buffers and some times they are called as data amplifier

* They are controlled by two signals namely. DEN and DT/R

* The DEN signal indicates the direction of data. i.e. from (or) to the processor.



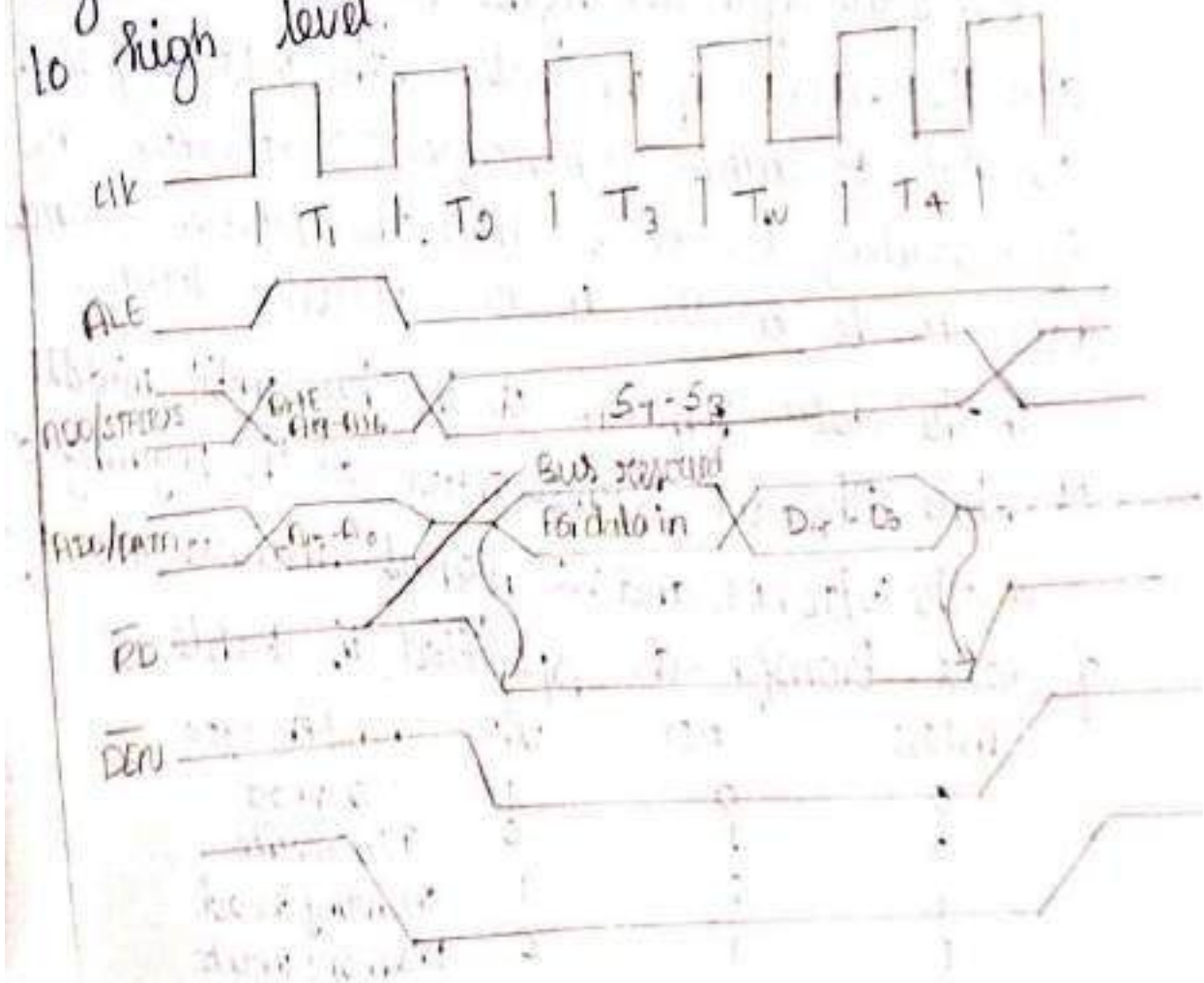
Bus timing for Minimum Mode :-

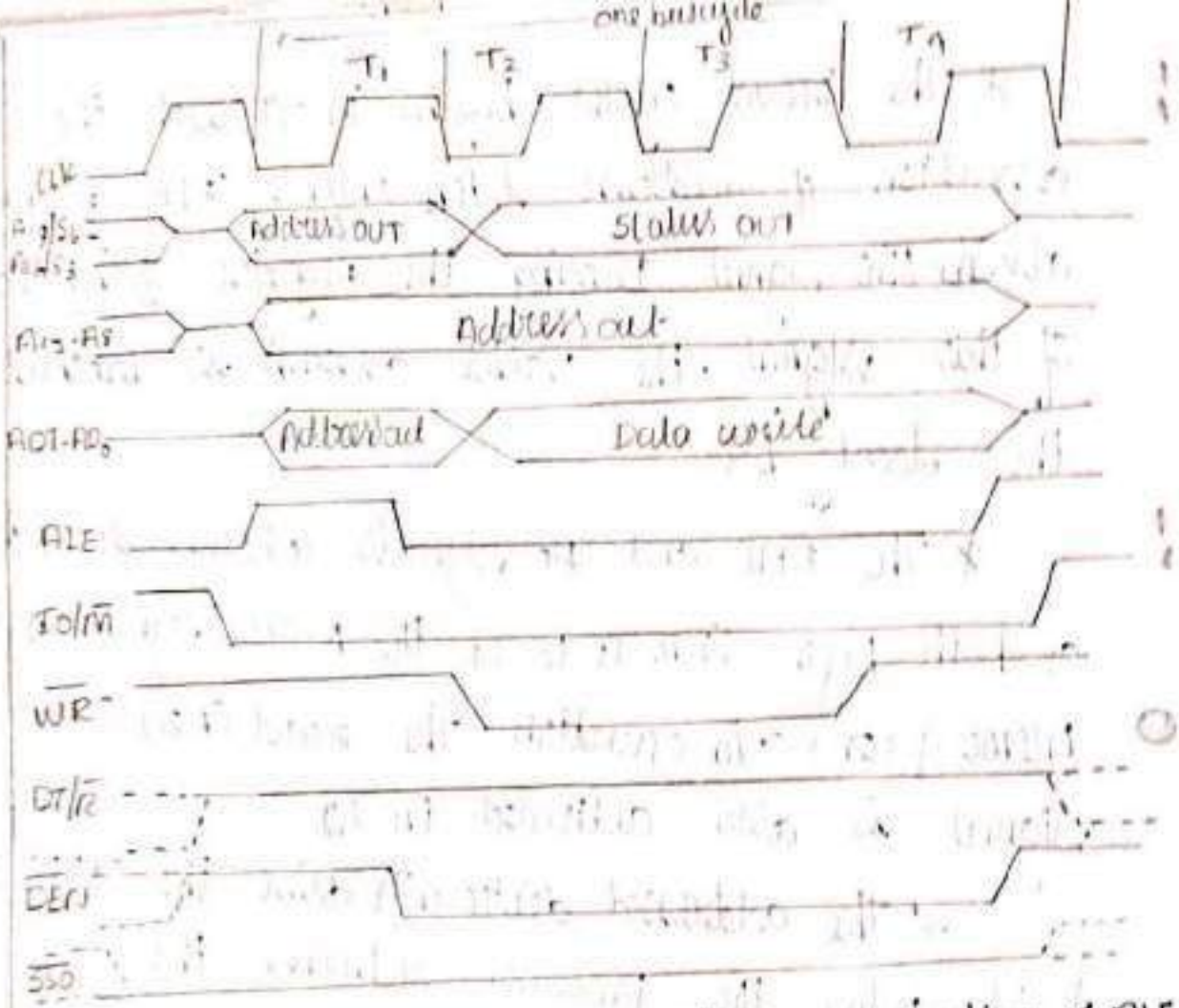
* The opcode fetch and read cycles are similar. Hence the timing diagram can be categorized in two parts, the first is the timing diagram for read cycle and the second is the timing diagram for write cycle.

* The read cycles begins in T_1 with the assertion of address latch enable (ALE) signal and also M/IO signal. During the negative going edge of this signal, the valid address is latched on the local bus.

* The BHE and A0 signals address low, high or both bytes from T_1 to T_4. The M/IO signal indicates memory (or) I/O operation. The read (RD) control signal is also activated in T_2.

* The addressed device will drive the READY line high when the processor returns the read signal to high level.





*A write cycle also begins with the assertion of ALE and the emission of the address. The IO/IO signal is again asserted to indicate a memory (or) I/O operation. In T2, after sending the address in T1, the processor sends the data to be written to the addressed location.

*The data remains on the bus until middle of T4 state. The WR becomes active at the begining of T2.

*The IO/IO, RD and WR signals indicate the type of data transfer as specified in table.

IO/IO	$\overline{RD}$	$\overline{WR}$	Transfer Type
0	0	1	I/O read
0	1	0	I/O write
1	0	1	Memory read
1	1	0	Memory write

Micro Processor &
Micro Controller

Assignment - 3

10

by.

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if one of the column bits has a zero, this means that a key press has occured. for example, if D3-D0 = 1101. this means that a key in the D1 column has been Pressed.

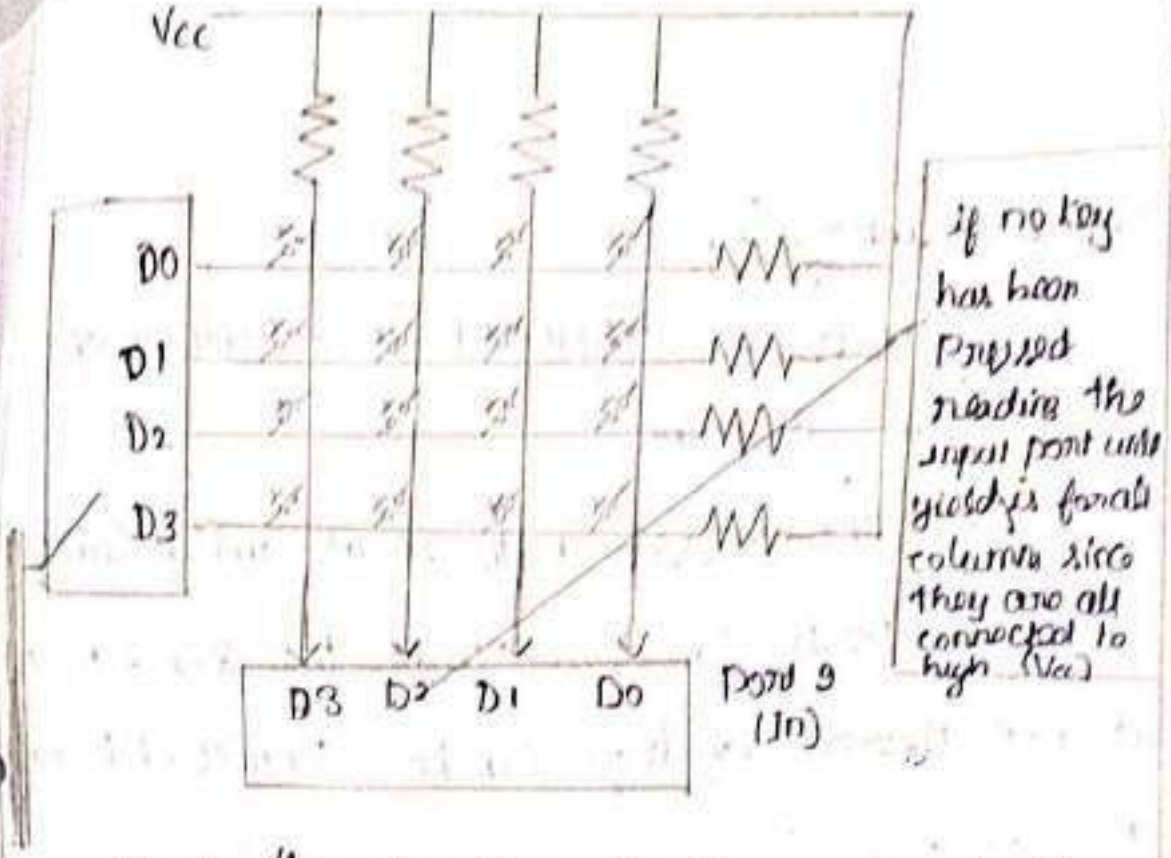
After detecting a key press, microcontroller will go through the process of identifying the key starting with the top row, the microcontroller grounds it by providing a low to row D0 only.

it reads the columns. if the data read is all is. no key in the row is activated and process is moved to the next row

it grounds the next row.

reads the columns, and checks for any zero

Find out which column the Pressed key belongs to



it is the function of the microcontroller to scan the keyboard continuously to detect and identify the key pressed To detect a pressed key, the microcontroller grounds all rows by proving 0 to the output latch, then it reads the columns.

if the data read from columns is D3 - D0 = 1111, no key has been pressed and the process continues till key press is detected.

If one of the column bits has a zero, this means that a key press has occurred.

Keyboard interfacing

Keyboards are organized in a matrix of rows and columns.

The CPU accesses both rows and colums through ports. Therefore, with two 8-bit ports, an 8×8 matrix of keys can be connected to 9 microprocessor.

when a key is pressed, a row and a column make a contact. otherwise, there is no connection between rows and columns.

In IBM PC keyboards, a single micro controller takes care of hardware and software interfacing. A 4×4 matrix connected to two ports.

The rows are connected to two output port & the column are to an input port KEYBOARD.

Micro Processors
Micro Controller

Assignment - 4

(10)

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I/O ports Pins, and Circuits

* 8051 microcontroller has 4 I/O ports. Each port has 8 bits which can be used as Input / output port Total 32 I/O pins are available.

* Each port has bi-directional capability.

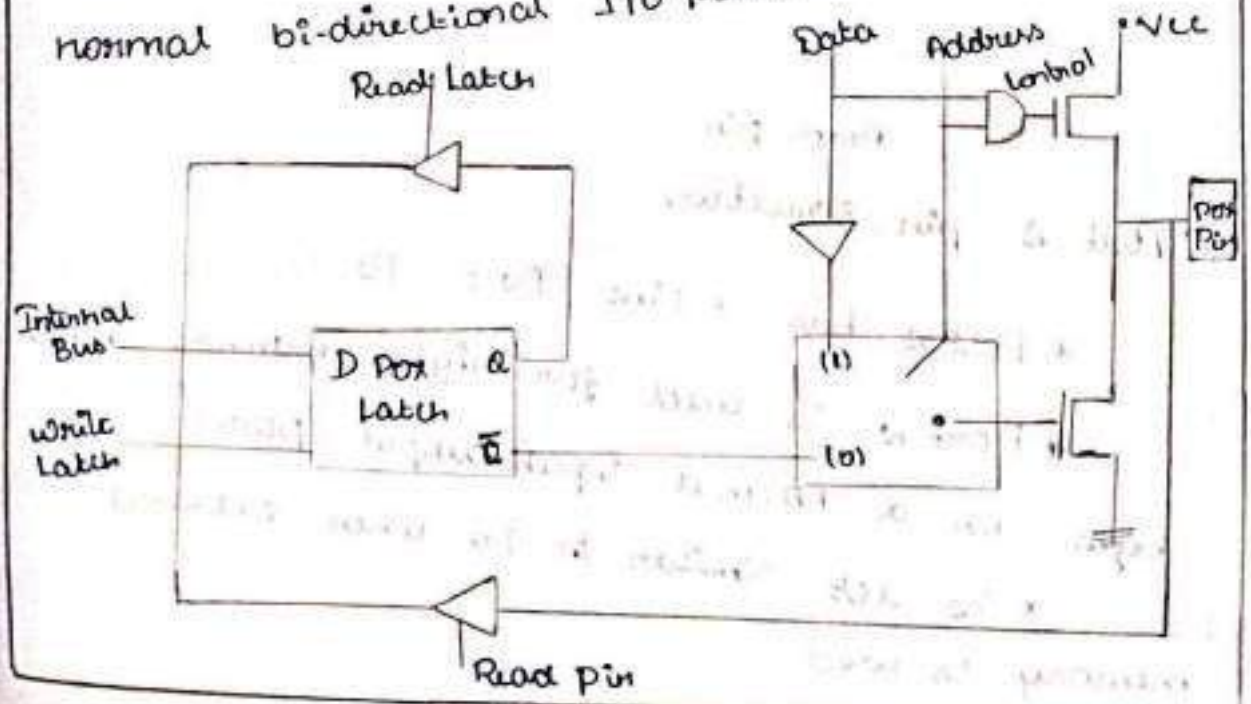
Port-0 - Pin Structure

* Port 0 has 8 pins

* Port 0 is called bi-directional port

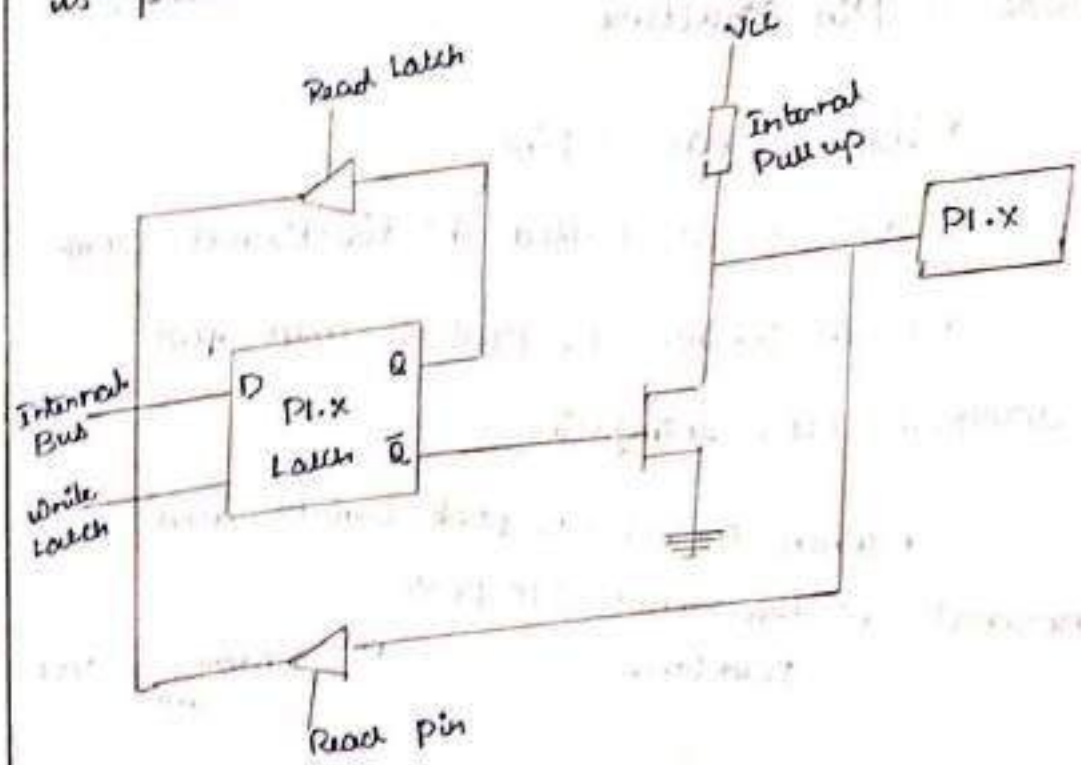
* When control = 1, port is used for address / data interfacing.

* When control = 0, port can be used as normal bi-directional I/O port.



Port - 1 Pin Structure

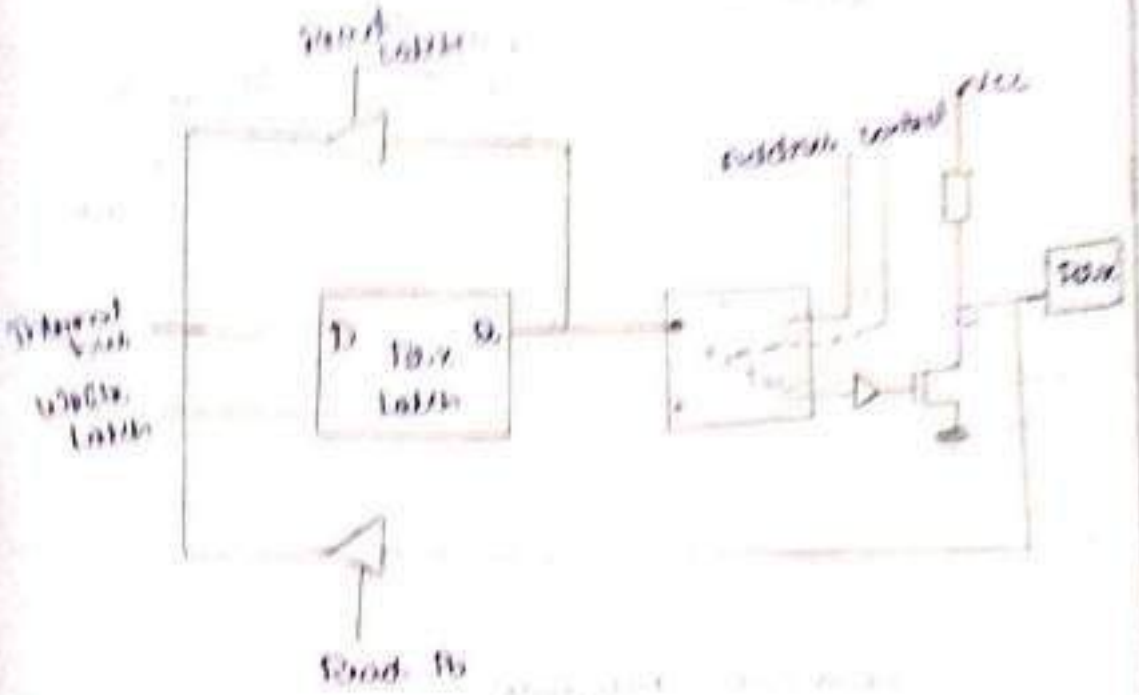
* Port 1 has 8 pins (P1.0 - P1.7)
* P1 is a true I/O port. because it doesn't have any alternative functions
* It has a pull-up register built-in
* When used as output port, the pin is pulled up (or) down



Port - 2 pin structure

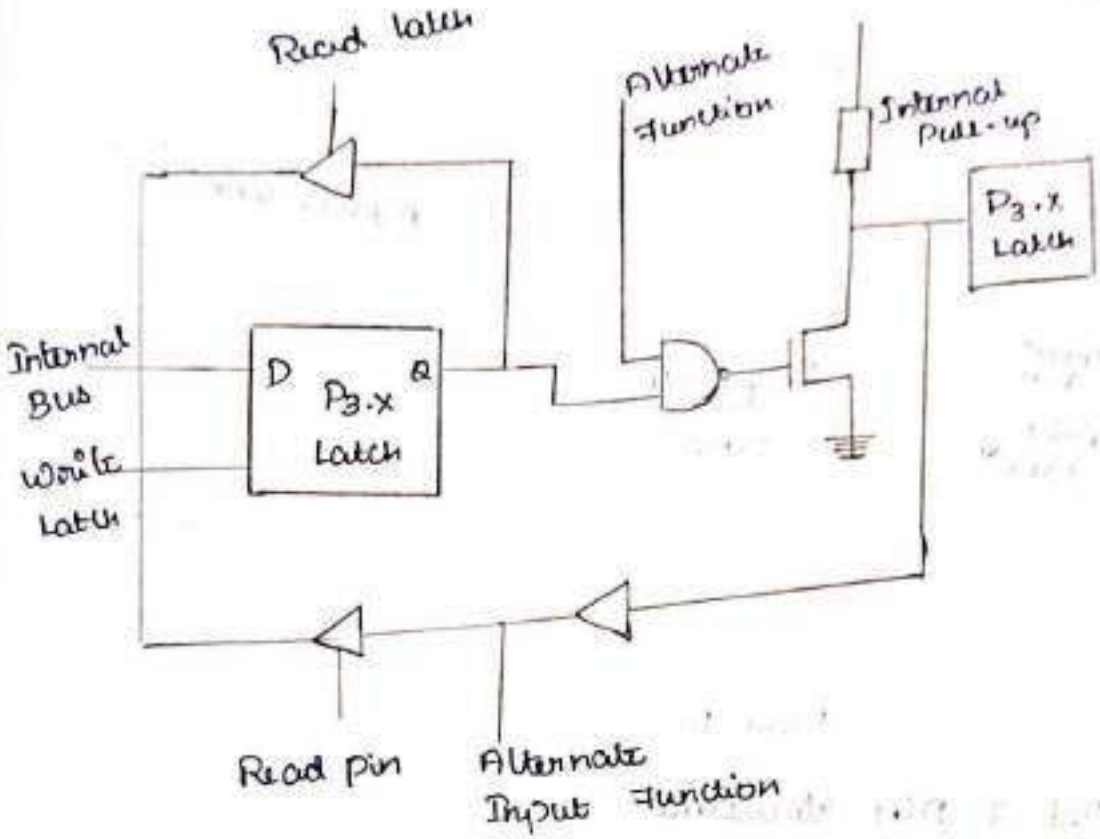
* Port 2 has 8 pins (P2.0 - P2.7)
* Port 2 is used for higher external address byte or a normal input/output port.
* P2 acts similar to P0 when external memory is used.

* When no memory is attached to port 0 it can be used as general I/O port



Port 3 pin structure

* Port 3 has 8 pins ($P_{3.0} - P_{3.7}$)
* Port 3 pins have alternate functions
* All ports can be used as general I/O pins they have alternate function
* To use the port as input port it should be written to the latch



Alternate functions.

$P_{3.7}$	$P_{3.6}$	$P_{3.5}$	$P_{3.4}$	$P_{3.3}$	$P_{3.2}$	$P_{3.1}$	$P_{3.0}$
RD	WR	T_1	T_0	INT1	INT0	TXD	RXD

MICROPROCESSOR AND MICROCONTROLLER

ASSIGNMENT - 5

10

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Steper motor interfacing with 8051 Microcontroller

This is basically a high voltage, high current Darlington transistor array. It has ULN2003 is used and each ULN2003 has Seven NPN Darlington pairs It can provide high voltage output with common cathode clamp diodes for switching inductive loads

Steper motor Interfacing

Steper motor is a Brushless DC electric motor that divides the complete rotation into very small angles called steps, Usually each step moves 1.8 degree and therefore a total of

200 steps for a rotor finish a single rotation. Unl normal DC- motors, It contains multiple Stator magnets used to trigger each step. Also each Stepper motor will have some fixed step angle and also the motor rotates at this angle

Stepper motor

The stepper motors are widely used in industrial and commercial applications also they are also commonly used as in drive system of autonomous robots.

Unipolar Steppermotor

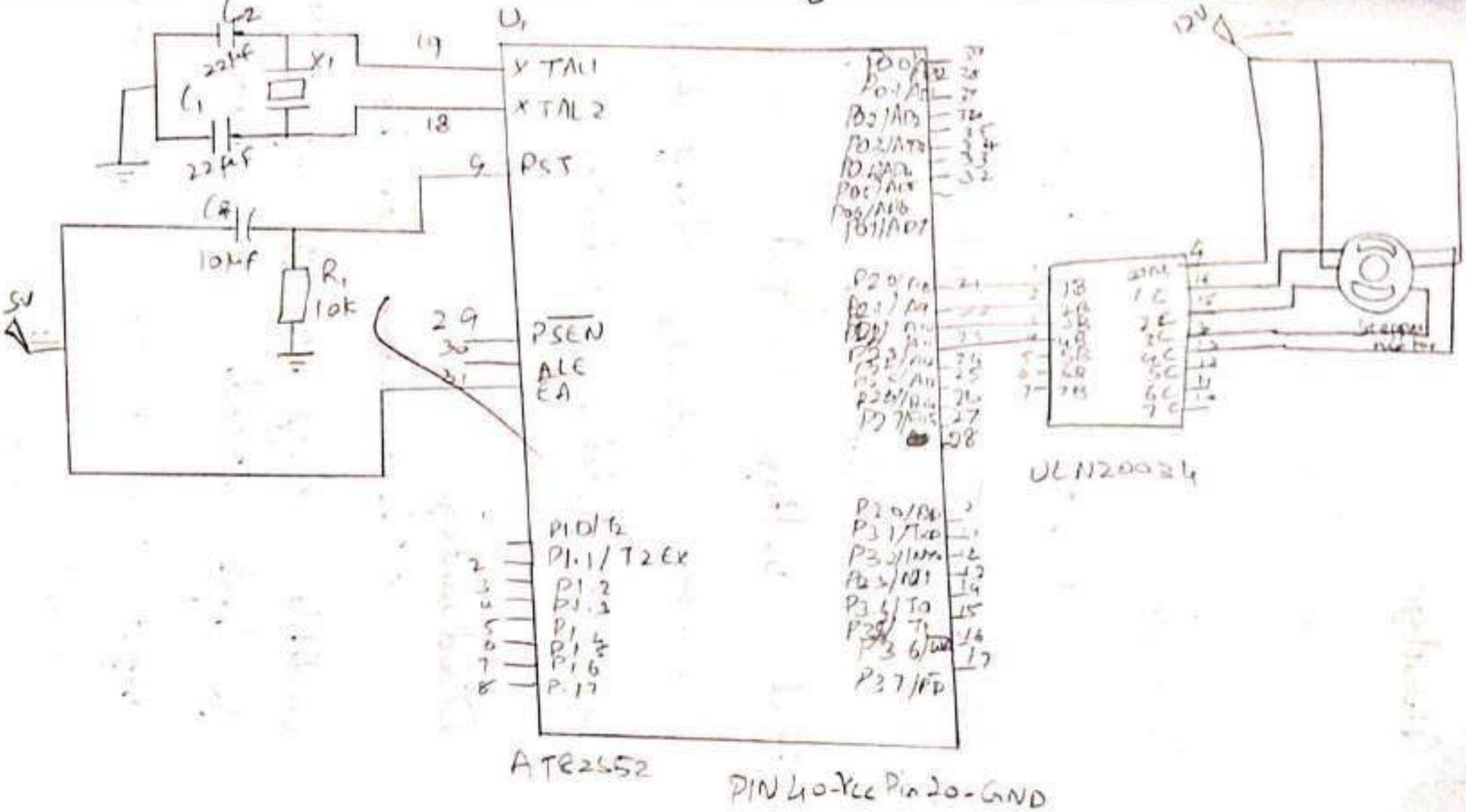
A two phase unipolar Stepper motor has a total of Six wires / leads of which four are each wires connected to coils stepper motor used here is green. Each common wire is connected to two end leads thus forming two phases the end leads corresponding to each phase Also these motors leads in a sequence is sufficient to drive the motor

Diagram of wave drive

Stepper motor

Signal sequence for wave drive Stepping mode				
Step	Yellow Lead	Blue Lead	Red Lead	White Lead
1	1	0	0	0
2	0	0	1	0
3	0	1	0	0
4	0	0	0	1

Circuit diagram



Advantage:

* This is basically in a high voltage.
* It has high Current Darlington transistor array
* It can provides high voltage output with common Cathode clamp diodes for switching inductive load.

Disadvantage.

* These motor can be audible very noisy at moderate to high speeds and have low output Power for Size and weight.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MODEL EXAMINATION

Subject Code: EC8551

Subject Name: COMMUNICATION NETWORKS

Time

Year/Branch :III/6

Part: A(5*2=10)

Q.No	COs	Cognitive Level	Questions
1	CO1	K1	Draw the flag register format of 8086 ?
2	CO1	K2	Calculate the physical address, when segment address is 1085 H and effective address is 4537 H.
3	CO2	K1	List the advanced microprocessors.
4	CO2	K1	What is main programming ? ?
5	CO3	K3	In an 8686 microprocessor, the contents of the accumulator and the carry flag are A7 (in hex) and 0,respectively . If the instruction RLC is executed ,then the contents of the accumulator (in hex) and the carry flag, respectively will be--- ---(GATE-2016)
6	CO3	K1	List the four display modes of 8279 keyboard/ display controller
7	CO4	K1	Give the alternate function for the port pins of port 3?
8	CO4	K1	Name the special functions registers available in 8051?
9	CO5	K1	Which register is used for serial programming in 8051? Illustrate it.
10	CO5	K2	Which register is used for serial programming in 8056? Illustrate it

Part: B(5X13=65)

Q.No	COs	Cognitive Level	Questions
11(a)	CO1	K2	Explain the internal hardware architecture of 8086 microprocessor with neat diagram
			OR
11(b)	CO1	K2	Discuss the interrupts types of 8086 microprocessor?
12(a)	CO2	K3	Explain closely coupled and loosely coupled configuration?
			(or)
12(b)	CO3	K2	Draw and explain the minimum mode of 8086?

13(a)	CO3	K2	Explain D/A and A/D interfacing done with 8086 with an application.
			OR
13(b)	CO3	K2	Draw the functional mock diagram of 8254 timer and explain the different modes of operation
14(a)	CO4	K2	Explain the memory organization of 8051 microcontroller.
			OR
14(b)	CO4	K2	Draw the pin diagram of 8051 microcontroller and explain the function of pin.
15(a)	CO5	K2	Describe the difference modes of operation of timers/counters in 8051 with its associated register.
			OR
15(b)	CO5	K3	Draw the diagram to interface a stepper motor with 8051 microcontroller and explain. Write a 8051 assembly language program to run and the stepper motor in both forward and reverse direction with delay

Part: C(15X1=15)

Q.No	COs	Cognitive Level	Questions
16(a)	CO3	K3	Explain with neat block diagram the working of parallel communication interfacing chip.
			OR
16(b)	CO1	K4	(i) Write the assembly language program to transfer a block of data between memory locations. (ii) Write the assembly language program for counting the number of 1's in a register

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AVK Nagar,, Pottalkualm, Azhagappapuram P.O kanyakumari District-629 401

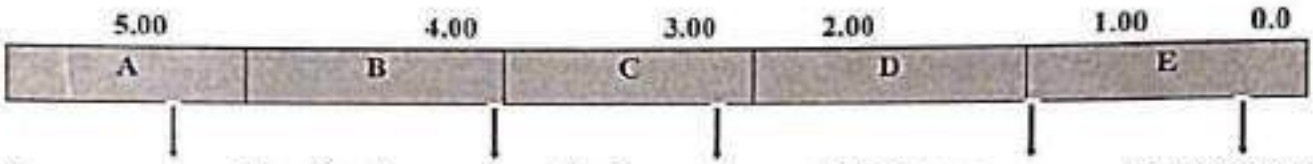
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Feedback Form

Semester / Year : 06/VI

Please rate the teachers on the following parameters using the 4 –point scale shown (A, B , C, D):

5	4	3	2	1	NA
Always	Often	Sometimes	Rarely	Never	"not Applicable" (I can't answer.)



Excellent Very Good Good Satisfactory Unsatisfactory

	Parameters	EC8094 (SC)	GE6075 (PE)
1.	Begins and ends our class on time.	4	4
2.	Is well-prepared for class.	5	5
3.	Clarity and understanding of the teachers explanation	5	5
4.	Knowledge of the teacher in subject	4	4
5.	Encourages students to ask questions and participate.	5	5
6.	Answers questions clearly.	5	5
7.	Teachers willingness to help	5	5
8.	Whether teacher dictates notes only without explanation	4	4
9.	Encourages me to think and explore new ideas.	4	4
10.	Tells the class at each meeting what we are going to do and what we are expected to learn.	5	5
11.	Treats all students respectfully.	5	5
12.	~~Whether teacher dictates notes only without explanation~~		
13.	Responds to my work so I know how I'm doing and what I need to work on.	4	4
14.	Speed of Presentation	3	3
15.	Promptness in valuation of tests and assignments	4	4
16.	Sincerity of the teacher	5	5
17	Study Materials is Clear and Understandable	3	4

Comments:

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AVK Nagar,, Pottalkualm, AzhagappapuramP.O.kanyakumari District-629 401

Date: 16 /03/2023

CIRCULAR FOR FIRST CLASS COMMITTEE MEETING

The First class committee meeting for the III-year ECE (6TH SEM) is scheduled on 17.03.2023 at 10.40 A.M in Simulation Lab. The following staff and students have to attend the meeting without fail.

CHAIR PERSON	Dr.Abilash
CONVENER	Mrs.P.Renuka
CLASS COORDINATOR	Mrs.E.Rajeswari
STAFF MEMBERS	Dr.Leonard Gibson
	Dr.A.Narendra Kumar
	Dr.Saheer Abubacker
	Dr.Supriya
	Dr.Vinoth
	Mr.R.Robert
STUDENT MEMBERS	A.Ahsan Akthar
	R.Santhiya

CHAIR PERSON

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Minutes of III Year Class Committee Meeting-I

Department of Electronics and Communication Engineering

Date of Meeting: 17-03-2023 **Time: 10.40 A.M-11.00A.M**

Members Present

1.Dr.Abilash , Professor/ECE	:	Chair Person
2.Mrs.P.Renuka , HoD, ECE	:	Convener
3.Mrs.E.Rajeswari AP/ECE	:	Class coordinator
4.Dr.Leonard Gibson Professor /ECE	:	Member
5.Dr.A.Narendra Kumar ,ASP/ECE	:	Member
6.Dr.Saheer Abubacker.ASP/ECE	:	Member
7. Dr.Supriya ASP/ECE	:	Member
8. Dr.Vinoth	:	Member
9.Mr.R.Robert	:	Member
10. A.Ahsan Akthar	:	Student Representative
11 R.Santhiya	:	Student Representative

The following matters were discussed in the meeting

1. The Students were instructed to be punctual for the class and maintain proper dress code.
2. The Student's feedback was received regarding the subjects.
3. The Students were asked to intimate their inconvenience to their concerned class coordinator.
4. The Students were advised to make use of seminar classes and placement hours effectively for improving their skills.
5. The Students were advised to be attentive in classes as well as laboratory classes.

HOD

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Date: 17/03 /2023

ATTENDANCE OF CLASS COMMITTEE MEETING-I

The following staff and students have attended the meeting on 17/03/2023.

S.NO.	NAME OF MEMBERS	SIGNATURE
1	Dr.Abilash	
2	Mrs.P.Renuka	
3	Mrs.E.Rajeswari	
4	Dr.Leonard Gibson	
5	Dr.A.Narendra Kumar	
6	Dr.Saheer Abubacker	
7	Dr.Supriya	
8	Dr.Vinoth	
9	Mr.R.Robert	

HOD/ECE

17/3/23

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Date: 19 /04 /2023

CIRCULAR FOR CLASS COMMITTEE MEETING-II

The second class committee meeting for the III-year ECE (6TH SEM) is scheduled on 21.4.2023 at 10.40 A.M in Simulation Lab. The following staff and students have to attend the meeting without fail.

CHAIR PERSON	Dr.Abilash
CONVENER	Mrs.P.Renuka
CLASS COORDINATOR	Mrs.E.Rajeswari
STAFF MEMBERS	Dr.Leonard Gibson
	Dr.A.Narendra Kumar
	Dr.Saheer Abubacker
	Dr.Supriya
	Dr.Vinoth
	Mr.R.Robert
STUDENT MEMBERS	A.Ahsan Akthar
	R.Santhiya

CHAIR PERSON

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Minutes of III Year Class Committee Meeting-II

Department of Electronics and Communication Engineering

Date of Meeting: 21-04-2023 **Time: 10.40 A.M-11.00A.M**

Members Present

1.Dr.Abilash , Professor/ECE	:	Chair Person
2.Mrs.P.Renuka , HoD, ECE	:	Convener
3.Mrs.E.Rajeswari AP/ECE	:	Class coordinator
4.Dr.Leonard Gibson Professor /ECE	:	Member
5.Dr.A.Narendra Kumar ,ASP/ECE	:	Member
6.Dr.Saheer Abubacker.ASP/ECE	:	Member
7. Dr.Supriya ASP/ECE	:	Member
8. Dr.Vinoth	:	Member
9.Mr.R.Robert	:	Student Representative
10. A.Ahsan Akthar	:	Student Representative
11 R.Santhiya		

The following matters were discussed in the meeting

1.Internal Assessment _I result analysis was discussed in the meeting.
2.The Student's feedback was received regarding the subjects and Lab.
3.Retest is decided for the absentees of IAT-I .
4.The Students were advised to make use of seminar classes and placement hours effectively for improving their skills.
5.The students are advised to keep their classrooms and surrounding clean.
6. Students are encouraged to participate in conferences and workshops.

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Date: 21/04 /2023

ATTENDANCE OF CLASS COMMITTEE MEETING-II

The following staff and students have attended the meeting on 21/04/2023.

S.NO.	NAME OF MEMBERS	SIGNATURE
1	Dr.Abilash	
2	Mrs.P.Renuka	
3	Mrs.E.Rajeswari	
4	Dr.Leonard Gibson	
5	Dr.A.Narendra Kumar	
6	Dr.Saheer Abubacker	
7	Dr.Supriya	
8	Dr.Vinoth	
9	Mr.R.Robert	

HOD/ECE

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Date: 16 /05 /2023

CIRCULAR FOR CLASS COMMITTEE MEETING-III

The third class committee meeting for the III-year ECE (6TH SEM) is scheduled on 19.5.2023 at 10.40 A.M in Simulation Lab. The following staff and students have to attend the meeting without fail.

CHAIR PERSON	Dr.Abilash
CONVENER	Mrs.P.Renuka
CLASS COORDINATOR	Mrs.E.Rajeswari
STAFF MEMBERS	Dr.Leonard Gibson
	Dr.A.Narendra Kumar
	Dr.Saheer Abubacker
	Dr.Supriya
STUDENT MEMBERS	Dr.Vinoth
	Mr.R.Robert
	A.Ahsan Akthar
	R.Santhiya

CHAIR PERSON

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Minutes of II Year Class Committee Meeting-III

Department of Electronics and Communication Engineering

Date of Meeting: 19-05-2023 **Time: 10.40 A.M-11.00A.M**

Members Present

1.Dr.Abilash , Professor/ECE	:	Chair Person
2.Mrs.P.Renuka , HoD, ECE	:	Convener
3.Mrs.E.Rajeswari AP/ECE	:	Class coordinator
4.Dr.Leonard Gibson Professor /ECE	:	Member
5.Dr.A.Narendra Kumar ,ASP/ECE	:	Member
6.Dr.Saheer Abubacker.ASP/ECE	:	Member
7. Dr.Supriya ASP/ECE	:	Member
8. Dr.Vinoth	:	Member
9.Mr.R.Robert	:	Member
10. A.Ahsan Akthar	:	Student Representative
11 R.Santhiya	:	Student Representative

The following matters were discussed in the meeting

1. Internal Assessment _2 result analysis was discussed in the meeting.
2. The Student's feedback was received regarding the subjects and Lab.
3. HoD enquired about the completion of lab experiments and records.
4. It was decided in the meeting to provide question bank with answers for all subjects.

HOD

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Date: 19/05 /2023

ATTENDANCE OF CLASS COMMITTEE MEETING-III

The following staff and students have attended the meeting on 19/05/2023.

S.NO.	NAME OF MEMBERS	SIGNATURE
1	Dr.Abilash	
2	Mrs.P.Renuka	
3	Mrs.E.Rajeswari	
4	Dr.Leonard Gibson	
5	Dr.A.Narendra Kumar	
6	Dr.Saheer Abubacker	
7	Dr.Supriya	
8	Dr.Vinoth	
9	Mr.R.Robert	

HOD/ECE

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PRINCIPAL 19/5/23

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

Department of Electronics & Communication Engineering

COURSE OUTCOME ATTAINMENT

Subject Code/ Name:	EC8691 / Microprocessors and Microcontr	Staff Nam	Mrs.P.Renuka	Batch :	2020-2024
Year/Sem :	III/6	BenchMark (%)	80	Number of Students in Class:	12

SLNo	Register Number	Name of the Student	M	Part A					Part B						CO Attainment(100%)		Number of Studnets Attained	Number of Studnets Attained
			Q.No.	1	2	3	4	5	6		7		8					
			Sub Div						a	b	a	b	a	b				
			Outcome	CO1	CO1	CO1	CO2	CO2	CO1	CO1	CO1	CO1	CO2	CO2				
			IA1 Mark	2	2	2	2	2	16	16	16	16	8	8	CO AD8501.1	CO AD8501.2	CO AD8501.1	CO AD8501.2
1	960120106001	AHSAN AKTHAR A	26	1		2		1		10		12			66	8	N	N
2	960120106002	GANGA V	24	1	1		1		8		8		5		47	50	N	N
3	960120106003	GANGA DEVI M	24	2		1	1			10		5	5		47	50	N	N
4	960120106004	MAKENTH R	4	2	2										11	0	N	N
5	960120106005	SANTHIYA R	31		2		2		12		10		5		63	58	N	N
6	960120106006	SIVARAJ S	9	2	2								5		11	42	N	N
7	960120106007	SREE VINISHA SHALINI P.S	31		2	2			12		10		5		68	42	N	N
8	960120106009	THANUSHA T.S	19	1		1		2		10				5	32	58	N	N
9	960120106303	BELWIN JOSHUA J	14				2	2	10						26	33	N	N
10	960120106305	KARTHICK	12	1			1				10				29	8	N	N
11	960120106306	SATHESSKUMAR C	17		1		1				10		5		29	50	N	N
12	960120106308	SUNDAR RAJA P	11		2		2			5			2		18	33	N	N
															Number of Students attained More than 80% of Marks		0	0
															% of CO Attainment		0.00	0.00
															attainment Level		0	0

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Department of Electronics & Communication Engineering

COURSE OUTCOME ATTAINMENT

INTERNAL ASSESSMENT II

Subject Code/ Name:	EC8691 / Microprocessors and Micr	Staff Nam	Mrs.P.Renuka	Batch :	2020-2024
Year/Sem :	III/6	Benchmark %	80	Number of Students in Class:	12

Sl.No	Register Number	Name of the Student	50	Part A					Part B						CO Attainment (100%)		Number of Studnets Attained	Number of Studnets Attained
			Q.No.	1	2	3	4	5	6		7		8					
			Sub Div						a	b	a	b	a	b				
			Outcome	CO2	CO2	CO3	CO3	CO3	CO2	CO2	CO3	CO3	CO3	CO3				
			EA3 Mark	2	2	2	2	2	16	16	16	16	80	80	CO AD8501.2	CO AD8501.3	CO AD8501.2	CO AD8501.3
1	960120106001	AHSAN AKTHAR A	29	2		1	1		10		10		5		60	57	N	N
2	960120106002	GANGA V	25		2	1		1		5		10		6	35	60	N	N
3	960120106003	GANGA DEVI M	31	2		2	2	2		8		12	3		50	70	N	N
4	960120106004	MAKENTH R	7				1	1					5		0	23	N	N
5	960120106005	SANTHIYA R	30	2		2	2	1	10		5		8		60	60	N	N
6	960120106006	SIVARAJ S	8	1	1	1				5					35	3	N	N
7	960120106007	SREE VINISHA SHALINI R S	33		2		2	2		10		12		5	60	70	N	N
8	960120106009	THANUSHA T S	23		1	2	2		10					8	55	40	N	N
9	960120106303	BELWIN JOSHUA J	31	2		2			12		10		5		70	57	N	N
10	960120106305	KARTHICK	14		2		2		10						60	7	N	N
11	960120106306	SATHESSKUMAR C	13	1		1	1			10					55	7	N	N
12	960120106308	SUNDAR RAJA P	18	1		1		1			10		5		5	57	N	N
															Number of Students attained More than 80% of Marks		0	0
															% of CO Attainment		0.00	0.00
															attainment Level		0	0

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Department of Electronics & Communication Engineering

COURSE OUTCOME ATTAINMENT

INTERNAL ASSESSMENT III

Subject Code/ Name:	EC8691 / Microprocessors and Microcontrollers	Staff Name:	Mrs.P.Renuka	Batch :	2020-2024
Year/Sem:	II/B	Benchmark %	80	Number of Students in Class:	12

Sl.No	Register Number	Name of the Student	Sq	Part A					Part B						Attainment (100%)		Number of Studnets Attained	Number of Studnets Attained
			Q.No.	1	2	3	4	5	6		7		8					
			Sub Div	a	b	a	b	a	b									
			Outcome	CO4	CO4	CO4	CO5	CO5	CO4	CO4	CO5	CO5	CO5	CO5				
			IA3 Mark	2	2	2	2	2	16	16	16	16	08	08	CO AD8501.4	CO AD8501.5	CO AD8501.4	CO AD8501.5
1	960120106001	AHSAN AKTHAR A	31	2		2		2	10		10		5		64	61	N	N
2	960120106002	GANGA V	35	2	2		1			12		10		8	73	68	N	N
3	960120106003	GANGA DEVI M	29	1		2	2	1		10		8	5		59	57	N	N
4	960120106004	MAKENTH R	6	1		1								4	9	14	N	N
5	960120106005	SANTHIYA R	34	2	2	2	1	1	10		8			8	73	64	N	N
6	960120106006	SIVARAJ S	11		1	1	1							8	9	32	N	N
7	960120106007	SREE VINISHA SHALINI P.S	36		2	2	2	1		12		12	5		73	71	N	N
8	960120106009	THANUSHA T.S	19	1	1	1	1				10		5		14	57	N	N
9	960120106503	BELWIN JOSHUA J	26	2	2			2	10		10				64	43	N	N
10	960120106305	KARTHICK	12					2			5		5		0	43	N	N
11	960120106306	SATHESSKUMAR C	18		1			2	5		10				27	43	N	N
12	960120106308	SUNDAR RAJA P	12			1	1				10				5	39	N	N
															Number of Students attained More than 80% of Marks		0	0
															% of CO Attainment		0.00	0.00
															attainment Level		0	0

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Department of Electronics & Communication Engineering
COURSE OUTCOME ATTAINMENT
MICRO LEVEL ANALYSIS

Subject Code / Name	EC 8691 - Microprocessors and Microcontrollers	Staff Name	Mrs. P. Nivetha
Year / Sem	III/V	Number of Students in Class	31
Batch	2020-2024	Batch Mark	

S. No.	Register Number	Name of the Student	IAT1+IAT2+IAT3 (Micro 1)										Assignment+Seminar (Micro 2)										University Result (Mapped)			Course End Survey (CES)					Bench Mark Attainment				
			CO1 Marks	Attainment Status	CO2 Marks	Attainment Status	CO3 Marks	Attainment Status	CO4 Marks	Attainment Status	CO5 Marks	Attainment Status	Ass 1 CO1	Attainment Status	Ass 2 CO2	Attainment Status	Ass 3 CO3	Attainment Status	Seminar CO4	Attainment Status	Ass 4 CO5	Attainment Status	Grade		Attainment Status	CO1	CO2	CO3	CO4	CO5	CO1	CO2	CO3	CO4	CO5
1		MOHAN AKTHAR A	64	N	54	N	57	N	64	N	61	N	80	Y	80	Y	70	N	70	N	80	Y	A	8	Y	60	60	80	70	60	1	1	2	2	1
2		GANGA V	47	N	43	N	60	N	73	N	68	N	90	Y	90	Y	80	Y	80	Y	90	Y	A+	9	Y	60	80	80	70	80	1	2	2	2	2
3		GANGA DEVI M	47	N	52	N	70	N	59	N	57	N	100	Y	100	Y	90	Y	90	Y	90	Y	A	8	Y	70	60	80	80	80	2	1	2	2	2
4		MAKENTHR	11	N	0	N	23	N	9	N	28	N	90	Y	90	Y	70	N	70	N	90	Y	U	0	N	80	70	60	60	60	2	2	1	1	1
5		SANTHIYA R	63	N	59	N	80	N	73	N	64	N	80	Y	80	Y	80	Y	80	Y	90	Y	A+	9	Y	70	70	60	60	60	2	2	1	1	1
6		SIVARAJ S	11	N	38	N	3	N	9	N	52	N	100	Y	100	Y	90	Y	90	Y	100	Y	B	6	N	80	90	70	90	70	2	3	2	3	2
7		VALLI UNNISA SHALINI S	68	N	51	N	70	N	73	N	71	N	100	Y	100	Y	90	Y	90	Y	90	Y	B+	7	N	70	80	80	90	80	2	3	2	3	2
8		THANUSHA T S	32	N	57	N	40	N	14	N	57	N	80	Y	80	Y	90	Y	90	Y	90	Y	A	8	Y	90	90	90	80	70	3	3	3	2	2
9		DELWIN JOSHUA J	26	N	52	N	57	N	64	N	43	N	75	N	90	Y	80	Y	90	Y	75	N	U	0	N	70	80	80	90	90	2	2	2	3	3
10		KARTHICK	29	N	38	N	7	N	0	N	43	N	75	N	90	Y	70	N	100	Y	80	Y	U	0	N	60	70	60	90	90	3	2	2	3	3
11		SATHEESSEKAR C	29	N	53	N	7	N	27	N	63	N	70	N	100	Y	80	Y	90	Y	90	Y	B	6	N	70	90	60	70	80	2	3	1	2	2
12		SUNDAR RAJA P	38	N	19	N	57	N	5	N	19	N	90	N	90	Y	75	N	90	Y	90	Y	U	0	N	60	70	60	80	80	1	2	1	2	2
Number of Students attained More than 60% of Marks			6		6		6		6		6		8		12		8		10		11				5									
% of attainment			0.5		0.5		0.5		0.5		0.5		66.7		100.0		66.7		83.3		91.7				41.7									
Attainment Level			0		0		0		0		0		2		3		2		3		3				0									
Average of Micro 1		0.60											Average of MICRO Assignment								2.6				End Term		0.8							

C	5
O	10
A+	9
A	8
B+	7
B	6
RA	0
U	0

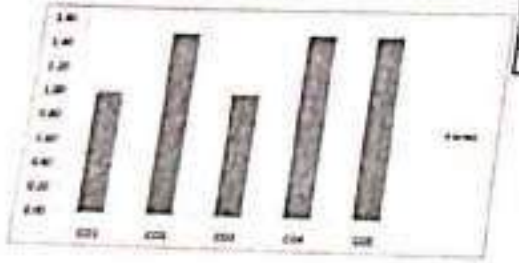
0	Attained O
1	Attained A+
2	Attained A
3	Attained B+
4	Attained B
5	Attained U
6	Attained C
12	Total

CO1	2.00
CO2	2.50
CO3	2.00
CO4	2.50
CO5	2.50

Direct CO Attainment = 20 % of IAT Direct + 10 % of Assignment Direct + 80 % of University	
20 % of IAT Direct	0.80
10 % of Assignment Direct	0.66
80 % of University	0.66
Direct CO Attainment	0.38
Overall CO Attainment = 80% of Direct CO + 20% of End Survey	
80 % of Direct CO	0.31
20 % of End Survey	0.31
Overall CO Attainment	0.62

COURSE END SURVEY				
CO/ LEVELS	1	2	3	CO %
CO1	4	7	1	75
CO2	2	6	4	81.25
CO3	4	7	1	75
CO4	2	6	4	81.25
CO5	3	7	2	84.38
AVERAGE ATTAINMENT LEVEL				2.81

MICRO 1					
	CO1	CO2	CO3	CO4	CO5
<=50	0	0	0	0	0
>=51 <60	1	0	4	5	4
>=60 <80	0	6	0	1	2
>=80	6	6	6	6	6



PRINCIPAL
ANNAI VAILANKANNI COLLEGE OF ENGINEERING
POTTALKULAM
AZHAGAPPAPURAM - 629401
KANYAKUMARI DIST.

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

PO-CO MAPPING

	SUBJECT CODE &	/ Microprocessors and Microcon			
BATCH		YEAR		BRANCH	ECE
ACADEMIC YEAR		2022-2023			

OVERALL CO ATTAINMENT	0.62

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
1	2	2	2	1	0	0	0	0	0	0	0	0	1	2
2	3	2	2	1	0	0	0	0	0	0	0	0	1	2
3	3	2	2	1	0	0	0	0	0	0	0	0	1	2
4	3	2	2	1	0	0	0	0	0	0	0	0	1	2
5	3	2	2	1	0	0	0	0	0	0	0	0	1	2
CO	2.80	2.00	2.00	1.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	1.00	2.00

PO-CO ATTAINMENT

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
1	0.41	0.41	0.41	0.21	0	0	0	0	0	0	0	0	0.21	0.41
2	0.62	0.41	0.41	0.21	0	0	0	0	0	0	0	0	0.21	0.41
3	0.62	1.38	0.41	0.21	0	0	0	0	0	0	0	0	0.21	0.41
4	0.62	0.41	0.41	0.21	0	0	0	0	0	0	0	0	0.21	0.41
5	0.62	0.41	0.41	0.21	0	0	0	0	0	0	0	0	0.21	0.41
CO	0.58	0.61	0.41	0.21	0	0	0	0	0	0	0	0	0.21	0.41

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PUTTALKULAM
AZHAGAPPAPURAM - 629 101
KANYAKUMARI DIST.

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

Azhagappapuram.P.O, K.K.District ,Tamil Nadu - 629 401

Department of Electronics and Communication Engineering W.e.f.-18-FEB 2023

UG TIME TABLE - 2022 to 2023 (EVEN)

Class : III YEAR Sem. : 06

HRS	1	2	BREAK	3	4	LUNCH BREAK	5	6	7
DAY	9.00 - 9.50	9.50 - 10.40		10.50-11.40	11.40-12.30		1.00-1.50	2.00-2.50	2.50-3.40
DAY 1									
DAY 2									
DAY 3									
DAY 4									
DAY 5							MPMC LAB	MPMC LAB	

LABORATORY CLASSES				
7	EC8681	Microprocessors and Microcontrollers Lab (MPMC LAB)	P	Mrs.P.Renuka

HOD

Date :

Principal

Date :

PRINCIPAL
ANNAI VAILANKANNI COLLEGE OF ENGINEERING
PUTTALADAM
AZHAGAPPAPURAM - 629 401
KANYAKUMARI DIST.

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

Azhagappapuram.P.O, K.K.District ,Tamil Nadu - 629 401

Department of Electronics and Communication Engineering W.e.f.-18-FEB 2023

UG TIME TABLE - 2022 to 2023 (EVEN)

Class : III YEAR Sem. : 06

HRS	1	2	BREAK	3	4	LUNCH BREAK	5	6	7
DAY	9.00 - 9.50	9.50 - 10.40		10.50-11.40	11.40-12.30		1.00-1.50	2.00-2.50	2.50-3.40
DAY 1									
DAY 2									
DAY 3									
DAY 4									
DAY 5							MPMC LAB	MPMC LAB	

LABORATORY CLASSES

7	EC8681	Microprocessors and Microcontrollers Lab (MPMC LAB)	P	Mrs.P.Renuka

HOD

Date :

Principal

Date :

PRINCIPAL
ANNAI VAILANKANNI COLLEGE OF ENGINEERING
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KANYAKUMARI DIST

222

IAT I

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

AVK Nagar, Pattukkottai, Kanyakumari 623 401

Department of Electronics and Communication Engineering

IAT I

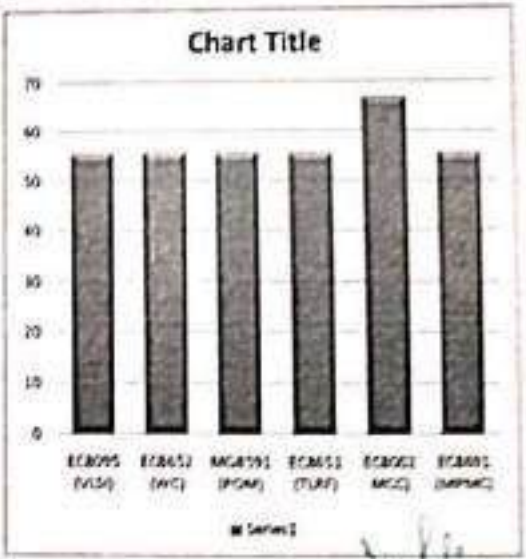
BATCH: 2020-2024 **YEAR: III** **STRENGTH: 9**

Sl No.	Reg. Number	Name of the Student	Subject Code						Number of subjects Passed	Number of Subjects AB	No. of Hours
			11 Sep	14 Sep	20 Sep	25 Sep	21 Sep	12 Sep			
			EC8095 (VLSI)	EC8652 (WC)	MG8591 (POM)	EC8651 (TLRF)	EC8652 (WC)	EC8691 (MPMC)			
1	[redacted]	ARAVAN AKILESH A	34	6	82	89	61	89	5	-	[redacted]
2	[redacted]	[redacted]	60	81	88	86	78	86	-	-	86
3	[redacted]	[redacted]	56	82	90	72	64	72	-	-	72
4	[redacted]	[redacted]	48	22	58	56	24	25	1	2	48
5	[redacted]	[redacted]	80	90	74	84	77	85	-	-	77
6	[redacted]	[redacted]	36	2	12	48	48	11	4	2	48
7	[redacted]	[redacted]	60	78	84	82	68	76	-	-	76
8	[redacted]	[redacted]	56	88	64	76	61	79	-	-	79
9	[redacted]	[redacted]	48	20	48	48	24	31	4	2	48

Subject Code	EC8095 (VLSI)	EC8652 (WC)	MG8591 (POM)	EC8651 (TLRF)	EC8652 (WC)	EC8691 (MPMC)
No of Students Appeared	7	9	7	8	8	9
No of Students Failed	2	4	2	3	2	4
No of Students Absent	2	0	2	1	1	3
Total No. Of students	9	9	9	9	9	9
No of Students Passed	5	5	5	5	6	5
Pass Percentage	56	56	56	56	67	56

Total no of Students	9
No of Students Passed in All Subjects	5
Overall Pass Percentage	55.6

S.No	SUBJECT CODE	NAME OF THE SUBJECT	FACULTY ALLOTED	% of Mark
1	EC8095 (VLSI)	VLSI Design	Mrs.T.Rajeswari	56
2	EC8652 (WC)	Wireless communication	Dr. Sujeiya	56
3	MG8591 (POM)	Principle of Management	Dr. Vinoth	56
4	EC8651 (TLRF)	Transmission Lines and RF Systems	Dr. Leonard Gibson	56
5	EC8652 MCC)	Multimedia Compression and Communication	Mr. R.Robert	67
6	EC8691 (MPMC)	Microprocessors and Microcontroller	Mrs.P.Renuka	56



FACULTY ADVISOR

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PATTUKKOTTAI
AZHAKIYAPANDIAPURAM - 629 401
KANYAKUMARI DIST.

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

AVK Nagar, Pottalkulam, Kanyakumari-629 001

Department of Electronics and Communication Engineering

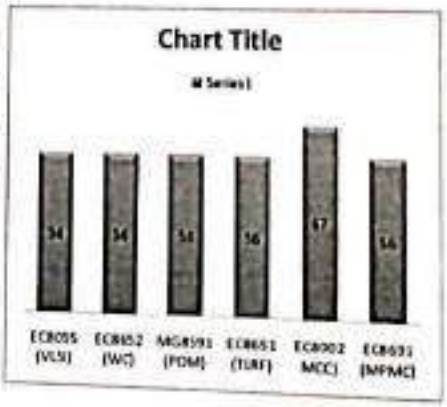
IAT II

BATCH: 2020-2024 **YEAR: III** **STRENGTH: 9**

Sl No	Reg. Number	Name of the Student	Subject Code						Number of subjects Failed	Number of subjects AB	% of Mark
			12-Oct	10-Oct	11-Oct	11-Oct	12-Oct	10-Oct			
			EC8095 (VLSI)	EC8652 (WC)	MG8591 (POM)	EC8651 (TLRF)	EC8002 MCC)	EC8691 (MPMC)			
1	[redacted]	AHSAN AKTHAR A	36	50	30	50	32	41	3	-	Fail
2	[redacted]	GANGA U	76	84	82	78	88	66	-	-	95
3	[redacted]	GANGA PRIYA M	62	90	70	68	90	55	-	-	87
4	[redacted]	MAKINI M	6	0	AB	0	AB	AB	3	3	AB
5	[redacted]	SANCHIYA R	74	86	82	88	74	76	-	-	94
6	[redacted]	SIVARAJ S	2	4	4	2	12	3	5	-	Fail
7	[redacted]	SREE VINDHA SHALINI P S	72	80	66	64	84	50	-	-	83
8	[redacted]	THANUSHA T S	62	82	80	76	64	66	-	-	86
9	[redacted]	SATHEESH KUMAR C	2	20	6	4	AB	9	5	-	Fail

Subject Code	EC8095 (VLSI)	EC8652 (WC)	MG8591 (POM)	EC8651 (TLRF)	EC8002 MCC)	EC8691 (MPMC)
No of Students Appeared	9	9	8	9	8	9
No of Students Failed	4	3	3	3	3	4
No of Students Absent	0	0	1	0	1	1
Total No. Of students	9	9	9	9	9	9
No of Students Passed	5	6	5	6	5	5
Pass Percentage	56	67	56	67	56	56

Total no of Students	9
No of Students Passed in All Subjects	5
Overall Pass Percentage	55.556



Sl No	SUBJECT CODE	NAME OF THE SUBJECT	FACULTY ADVISOR	% of Mark
1	EC8095 (VLSI)	VLSI Design	Mrs E Rajeswari	56
2	EC8652 (WC)	Wireless communication	Dr Supriya	67
3	MG8591 (POM)	Principle of Management	Dr. Vinoth	56
4	EC8651 (TLRF)	Transmission Lines and RF Systems	Dr. Leonard Gnana	56
5	EC8002 MCC)	Multimedia Compression and Communication	Mr. R.Robert	67
6	EC8691 (MPMC)	Microprocessors and Microcontroller	Mrs P Renuka	56

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POTTALKULAM
AZHAGAPPAPURAM
KANYAKUMARI DIST.

IAT 3

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

AVK Nagar, Pottalkulam, Kanyakumari 629 401

Department of Electronics and Communication Engineering

IAT III

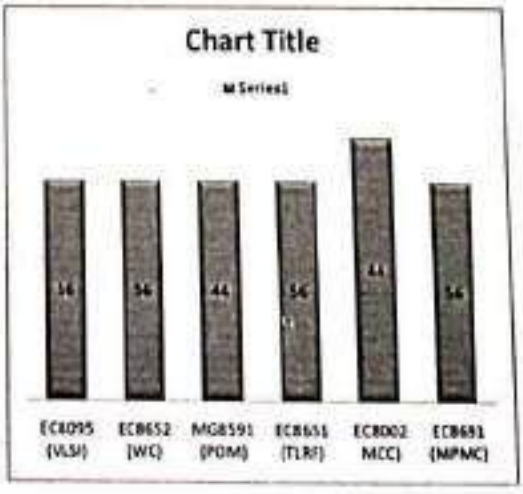
BATCH: 2020-2024 **YEAR: III** **STRENGTH: 9**

Sl.No	Reg. Number	Name of the Student	Subject Code						Number of subjects Failed	Number of Subjects AB	% of Mark
			12-Oct	10-Oct	11-Oct	11-Oct	10-Oct	10-Oct			
			EC8095 (VLSI)	EC8652 (WC)	MG8591 (POM)	EC8651 (TLRF)	EC8002 MCC)	EC8691 (MPMC)			
1	960120106001	AHSAN AKTHAR A	50	38	68	52	50	51	1	-	Fail
2	960120106002	GANGA V	78	96	72	58	84	75	-	-	93
3	960120106003	GANGA DEVESH	AB	54	AB	AB	90	AB	-	4	AB
4	960120106004	HAKENTH	AB	AB	20	AB	0	AB	1	4	AB
5	960120106005	SANTHIYA R	74	84	62	72	86	80	-	-	92
6	960120106006	SIVAPAL S	16	4	16	0	4	10	5	-	Fail
7	960120106007	SHEY VINISHA SHALINI P S	66	80	56	62	80	72	-	-	83
8	960120106008	THANUSHA T S	58	58	AB	AB	82	AB	-	3	AB
9	960120106406	VATHEESWARAN KUMAR C	AB	30	28	4	20	50	3	1	AB

Subject Code	EC8701 (AWSN)	EC8751 (OC)	EC8701 (AME)	EC8791 (ERTS)	OE751 (Robotics)	EC8691 (MPMC)
No of Students Appeared	9	9	8	9	8	9
No of Students Failed	1	3	3	2	1	4
No of Students Absent	3	1	2	3	3	3
Total No. Of students	9	9	9	9	9	9
No of Students Passed	5	5	4	4	5	5
Pass Percentage	56	56	44	44	56	56

Total no.of Students	9
No of Students Passed in All Subjects	3
Overall Pass Percentage	33.33

Sl.No	SUBJECT CODE	NAME OF THE SUBJECT	FACULTY ALLOTED	% of Mark
1	EC8095 (VLSI)	VLSI Design	Mrs.E.Rajeswari	56
2	EC8652 (WC)	Wireless communication	Dr. Supriya	56
3	MG8591 (POM)	Principle of Management	Dr. Vinoth	44
4	EC8651 (TLRF)	Transmission Lines and RF Systems	Dr. Leonard Gibson	56
5	EC8002 MCC)	Multimedia Compression and Communication	Mr. S.Robert	44
6	EC8691 (MPMC)	Microprocessors and Microcontroller	Mrs P.Renuka	56



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POTTALKULAM
AZHAGAPPAPURAM - 629 401
KANYAKUMARI DIST.

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

AVK Nagar, Pottalkulam, Kanyakumari 629 401

Department of Electronics and Communication Engineering

6th Sem University Exam Result Analysis

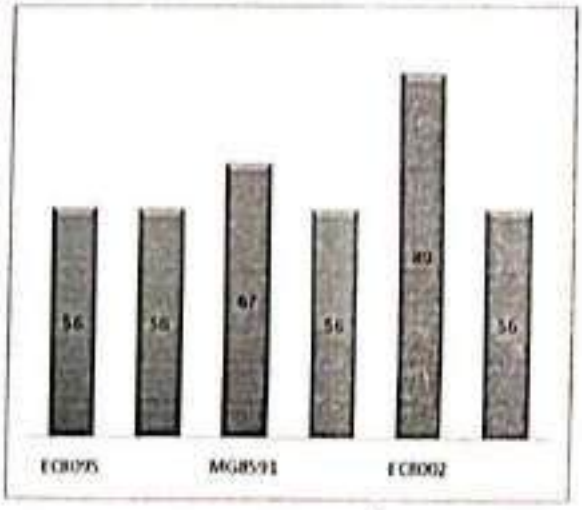
BATCH: 2020-2024 **YEAR: III / 6** **STRENGTH: 09**

Sl.No.	Reg. Number	Name of the Student	Subject Code						Number of subjects Failed	Number of Subjects AB	Number of Sub. Pass
			EC8095 (VLSI)	EC8652 (WC)	MG8591(POM)	EC8651 (TRT)	EC8002 (MCC)	EC8691 (MPMC)			
1	960120106001	AHSAN AKTHAR A	U	B	B+	U	A	U	3		3
2	960120106002	GANGA V	B	A	B+	B	A+	B+	-	-	6
3	960120106003	GANGA DEVEMI	B	A	B+	B	A	B+			6
4	960120106004	MARI NITH	U	UA	U	U	UA	UA	3	3	0
5	960120106005	NANDHIVA R	B	A	B+	B	A+	B+	-	-	6
6	960120106006	SIVARAJ S	U	UA	U	U	B	UA	3	2	1
7	960120106007	SOUNDARYA SHAGINEPS	B+	B	B+	B	B+	B+	-	-	6
8	960120106008	THANUSHA T S	B	U	B	B	A	B	1		5
9	960120106306	VAITHEESH KUMAR C	U	U	U	U	B	U	5	-	1

Subject Code	EC8095	EC8652	MG8591	EC8651	EC8002	EC8691
No of Students Appeared	9	7	9	9	8	7
No of Students Failed	4	2	3	4	0	2
No of Students Absent	0	2	0	0	1	2
Total No. Of students	9	9	9	9	9	9
No of Students Passed	5	5	6	5	8	5
Pass Percentage	56	56	67	56	89	56

Total no.of Students	9
No of Students Passed in All Subjects	4
Overall Pass Percentage	44.4

Sl.No	SUBJECT CODE	NAME OF THE SUBJECT	FACULTY ALLOTED	% of Mark
1	EC8095 (VLSI)	VLSI Design	Mrs.T.Rajeswari	56
2	EC8652 (WC)	Wireless Communication	Dr. Supriya	56
3	MG8591 (POM)	Principles of Management	Dr.Vinoth	67
4	EC8651 (TRT)	Transmission Lines and RF Systems	Dr.Leonard Gibson	56
5	EC8002 (MCC)	Multimedia Compression and Communication	Mr.R.Robert	89
6	EC8691 (MPMC)	Microprocessors and Microcontrollers	Mrs.P.Renuka	56



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ANNAI VAILANKANNI COLLEGE OF ENGINEERING
AZHAGAPPAPURAM - 629 301

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

AVK Nagar, Pothaiyadisalai, Pottalkulam,
Azhagappapuram Post, Kanyakumari District,
Tamilnadu - 629401.

ATTENDANCE
&
ASSESSMENT RECORD
(THEORY)

Year : 2022-23 [EVEN] Semester : 06

Class : III Year Branch : ECE

Name : Mrs. P. Remika

Department : Electronics and Communication

Code No. / Course Title : EC8691 - Microprocessors and Microcontrollers

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

AVK Nagar, Pothaiyadisalai, Pottalkulam,
Azhagappapuram Post, Kanyakumari District,
Tamilnadu - 629401.

ATTENDANCE
&
ASSESSMENT RECORD
(THEORY)

Year : 2022-23 [EVEN] Semester : 06

Class : III Year Branch : ECE

Name : Mrs. P. Remska

Department : Electronics and Communication

Code No. / Course Title : EC8691 – Microprocessors and Microcontrolleas

Class :

ATTENDANCE

Sl. No.	Roll No.	Name	Date	6	7	8	8	9	13	14	15	15	16
			Month	2	2	2	2	2	2	2	2	2	2
			Period	1	5	4	7	2	3	5	4	7	2
1.	20REC01	Ahsan Akthar . A		/	/	/	/	/	/	/	/	/	/
2.	20REC02	Ganga . V		/	/	/	/	/	/	/	/	/	/
3.	20REC03	Ganga Devi . M		/	/	/	/	/	/	/	/	/	/
4.	20REC04	Makenth . R		/	a	a	a	a	a	a	a	a	/
5.	20REC05	Santhiya . R		/	/	/	/	/	/	/	/	/	/
6.	20REC06	Siva Raj . S		/	/	a	a	/	a	a	/	/	/
7.	20REC07	Sri Vinisha Shalini . PS		/	/	/	/	/	/	/	/	/	/
8.	20REC08	Thanusha . T . S		/	/	/	/	/	/	/	/	/	/
9.	20LEC03	Belwin Joshwa . T		a	/	/	/	/	/	/	a	a	a
10.	20LEC04	Judeson Bino . B		/	/	/	/	a	/	/	/	/	/
11.	20LEC05	Karthick . N		/	/	/	/	/	/	/	/	/	/
12.	20LEC06	Sathesh Kumar . C		/	a	a	a	a	a	/	/	/	/
13.	20LEC07	Sneka . H		/	/	/	/	/	/	/	/	/	/
14.	20LEC08	Sundararaj . P		a	/	/	/	/	a	/	/	/	/

Signature of the Faculty

Signature of the HoD

ATTENDANCE

20	21	22	22	23	25	27	29	1	1
2	2	2	2	2	2	2	2	3	3
1	5	5	7	2	1	1	5	4	7
/	/	/	/	/	/	/	/	/	/
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229

Class :

Sl. No.	Roll No.	Name
1.	20REC01	Ahsan Akthar.
2.	20REC02	Ganga. V
3.	20REC03	Ganga Devi. J
4.	20REC04	Makenth. R
5.	20REC05	Santhiya. R
6.	20REC06	Siva Raj. S
7.	20REC07	Sri Vinisha Shal
8.	20REC08	Thanusha. T.S
9.	20LEC03	Belwin Joshua
10.	20LEC04	Judeson Bino
11.	20LEC05	Karthick. N
12.	20LEC06	Santhosh Kuma
13.	20LEC07	Sneka. H
14.	20LEC08	Sundararaj. F

Signature of the Faculty

Signature of the HoD

ATTENDANCE

2	6	7	8	8	9	11	11	13	15
3	3	3	3	3	3	3	3	3	3
2	1	5	4	7	2	4	7	1	4
/	/	/	/	/	/	/	/	/	/
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a	/	/	/	/	a	/	/	/	/

ATTENDANCE

15	16	19	20	21	23	27	28	29	29
3	3	3	3	3	3	3	3	3	3
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Class :

Sl. No.	Roll No.	Name
1.	20REC01	Ahsan Akthar.
2.	20REC02	Ganga. V
3.	20REC03	Ganga Devi. P
4.	20REC04	Makenth. R
5.	20REC05	Santhiya. R
6.	20REC06	Siva Raj. S
7.	20REC07	Sri Vinisha Shali
8.	20REC08	Thanusha. T.S
9.	20LEC03	Belwin Joshua
10.	20LEC04	Judeson Bino.
11.	20LEC05	Karthick. N
12.	20LEC06	Santhosh Kumar
13.	20LEC07	Sneka. H
14.	20LEC08	Sundararaj. P

Signature of the Faculty

Signature of the HoD

ATTENDANCE

30	1	1	3	5	5	6	10	11	12
3	4	4	4	4	4	4	4	4	4
2	5	7	1	4	7	2	1	5	4
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ATTENDANCE

12	13	17	18	19	19	20	24	25	26
4	4	4	4	4	4	4	4	4	4
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Class :

Sl. No.	Roll No.	Name	ATTENDANCE									
			26	27	29	2	3	3				
			4	4	4	5	5	5				
			7	2	2	5	4	7				
1.	20REC01	Ahsan Akthar.	/	/	/	/	a	a				
2.	20REC02	Ganga. V	/	/	/	/	/	/				
3.	20REC03	Ganga Devi. J	/	/	/	/	/	/				
4.	20REC04	Mahanth. R	/	/	/	/	/	/				
5.	20REC05	Santhiya. R	/	/	/	/	/	/				
6.	20REC06	Siva Raj. S	a	/	/	/	/	/				.
7.	20REC07	Sri Vinisha Shal	/	/	/	/	/	/				
8.	20REC08	Thanuska. T.S	/	/	/	/	/	/		.		
9.	20LEC53	Belwin Jaskins	/	a	/	/	/	/	.			
10.	20LEC04	Judeson Rins	/	/	/	/	.	/				
11.	20LEC05	Karthick. N	/	/	a	/	/	/				
12.	20LEC06	Sathish Kuma	/	/	/	/	/	/				
13.	20LEC07	Sneka. H	.	/	/	a	/	/			.	
14.	20LEC08	Sundararaj. F	/	/	/	a	/	/				.
Signature of the Faculty												
Signature of the HoD												

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Class : EC 8691 – Microprocessors and Microcontrollers

SUBJECT COVERAGE STATEMENT

Sl. No.	Date	Period	Topics Covered	Book Followed	Initials	
					Faculty	HoD
			UNIT – I			
1.	6/2/23	1	Introduction to 8086	T1		
2.	7/2/23	5	Microprocessor Architecture	T1		
3.	8/2/23	4/7	Addressing modes	T1		
4.	9/2/23	2	Instruction Set	T1		
5.	13/2/23	1	Assembler directives	T1		
6.	14/2/23	5	Assembly Language Programming	T1		
7.	15/2/23	4	Modular Programming	T1		
8.	15/2/23	7	Linking + Relocation	T1		
9.	16/2/23	2	Stacks – Procedures	T1		
10.	20/2/23	1	Macros – Interrupts	T1		
11.	21/2/23	5	Byte and String Manipulation	T1		

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Class :

SUBJECT COVERAGE STATEMENT

Sl. No.	Date	Period	Topics Covered	Book Followed	Initials	
					Faculty	HoD
			UNIT - II			
13.	22/2/23	5	8086 Signals	T_1		
14.	22/2/22	7	Basic Configuratims	T_1		
15.	23/2/22	2	System bus Timing	T_1		
16.	25/2/22	1	System design using 8086	T_1		
17.	27/2/23	1	I/O programming	T_1		
18.	28/2/23	5	Introductim to Multiprogramming	T_1		
19.	1/3/23	4	System bus structure	T_1		
20.	1/3/23	7	Multiprocessor Configuratims	T_1		
21.	2/3/23	2	Co-processor	T_1		
22.	5/3/23	1	closely + Loosely coupled	T_1		
23	7/3/23	5	Advanced processors	T_1		

Class :

SUBJECT COVERAGE STATEMENT

Sl. No.	Date	Period	Topics Covered	Book Followed	Initials	
					Faculty	HoD
			UNIT - III			
24.	8/3/23	4	Memory and I/O Interfacing	T1		
25	8/3/23	7	Parallel communicatim Interface	T1		
26	9/3/23	2	Serial Communicatim Interface	T1		
27.	11/3/23	4	D/A and A/D interface	T1		
28	11/3/23	7	Timer	T1		
29	13/3/23	1	keyboard / display Controller	T1		
30	15/3/23	4	Interrupt Controller	T1		
31	15/3/23	7	DMA Controller	T1		
32	16/3/23	2	Traffic light Control	T1		
33	18/3/23	2	LED display	T1		
34	20/3/23	1	LCD display	T1		
35	21/3/23	5	keyboard display interface	T1		
36.	23/3/23	2	Alarm controller	T1		

Class :

SUBJECT COVERAGE STATEMENT

Sl. No.	Date	Period	Topics Covered	Book Followed	Initials	
					Faculty	HoD
			UNIT-IV			
			Microcontroller			
37	27/3/23	1	Architecture of 8051	T2		
38	28/3/23	5	Architecture of 8051	T2		
39	29/3/23	4	Special function Registers	T2		
40	29/3/23	7	I/O pins	T2		
41	30/3/23	2	I/O ports + Circuits	T2		
42	1/4/23	5, 7	Instruction Set	T2		
43	5/4/23	4, 7	Addressing modes	T2		
44	6/4/23	2	Assembly Language Programming	T2		
45	10/4/23	5	Programming	T2		
46	11/4/23	5.	Programming.	T2.		

Class :

SUBJECT COVERAGE STATEMENT

Sl. No.	Date	Period	Topics Covered	Book Followed	Initials	
					Faculty	HoD
			UNIT-5			
			Interfacing Microcontroller			
47	12/4/23	4/7	Programming 8051 Timers	T2		
48	13/4/23	2	Serial port programming	T2		
49	17/4/23	1	Interrupts Programming	T2		
50	18/4/23	5	LCD & keyboard Interfacing	T2		
51	19/4/23	4/7	ADC, DAC	T2		
52	20/4/23	2	Sensor Interfacing	T2		
53	24/4/23	1	Stepper motor	T2		
54	25/4/23	5	Waveform Generation	T2		
55	26/4/23	4	Comparison of Microprocessor	T2		
56	26/4/23	7	Microcontrollers, PIC	T2		
57	27/4/23 29/4/23	2 2	ARM processors	T2		
58	2/5/23	5	Revision	T2		
59	3/5/23	4	Revision	T2		
60	3/5/23.	7	Revision	T2		

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Class :

SUBJECT COVERAGE STATEMENT

Sl. No.	Date	Period	Topics Covered	Book Followed	Initials	
					Faculty	HoD
	Text Books.					
	1. Yu-cheng Liu, Glenn A. Gibson - Microcomputer systems : The 8086/8088 Family - Architecture, Programming + Design'					
	2. Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin Mckinlay "The 8051 Microcontroller and Embedded systems : using Assembly + C"					

WEEKLY TEST

Subject : EC8691 MPMC Sem / Branch : 06 / ECE

Faculty : Mrs. P. Renuka

Roll No.	Student's Name	Marks			
		Date: Test No. 1	Date: ReTest No.	Date: Test No. 2	Date: Re Test No.
20REL01	Ahsan Akthar. A	65		78	
20REL02	Ganga. V	73		80	
20REL03	Ganga Devi. M	85		83	
20REL04	Makanth. R	32		50	
20REL05	Santhiya. R	80		72	
20REL06	Siva Raj. S	AB		26	
20REL07	Sri Vinisha Shalini. P. S	72		83	
20REL09	Thanusha. T. S	78		85	
20LEL03	Belwin Joshua. J	AB		50	
20LEL04	Judeson Bino. B	32		42	
20LEL05	Karthick. N	07		33	
20LEL06	Sathesh Kumar. C	52		54	
20LEL07	Sneka. H	87		89	
20LEL08	Sundararaj. P	33		AB	
	Signature of the Faculty				
	Signature of the HoD				

C.I.A. Sheet of Subjects

Class : III Year / 06 sem Branch : ECE

Faculty : Mrs. P. Renuka

Roll No.	Name	Test Marks (100)			Internal Marks 100 (Average of 3)
		Int 1	Int 2	Int 3	
20REL01	Ahsan Akthar. A	93	82	81	
20REC02	Ganga. V	100	90	92	
20REC03	Ganga Devi. M	100	83	89	
20REC04	Maksenth. R	78	76	75	
20REL05	Santhiya. R	100	86	93	
20REL06	Siva Raj. S	80	80	78	
20REC07	Sri Vinisha Shalini. P.S	87	93	95	
20REC09	Thanusha. T.S	100	92	93	
20LEC03	Belwin Joshua. J	76	72	71	
20LEC04	Judeson Bino. B	72	73	74	
20LEC05	karthick. N	70	56	64	
20LEC06	Sathesh kumar. C	85	65	62	
20LEC07	Sneka. H	100	92	80	
20LEC08	Sundararaj. P	74	93	96	
	Date of Exam :	18/3	17/4	15/5	
	Faculty :				
	Verification : HoD				
	Approval PRINCIPAL :				

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Time Table for the Academic Year 2022 - 2023
(Odd / Even Sem.)

Day Order	I	II	III	IV	V	VI	VII	VIII
Mon	MPMC							
Tue					MPMC			
Wed					M'pmc			
Thur		MPMC						
Fri								

			Tea Break					
			Tea Break					
			Tea Break					

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EXAM CELL

DATE: 10-03-2023

CIRCULAR

All faculty members are hereby informed that Internal Assessment Test-I will be held from 15-03-2023 to 20-03-2023

Exam Cell

10/3/23

Principal

Copy To:

- The Chairman
- The Director
- Vice –Principal
- All HODs

ANNAI VAILANKANNI COLLEGE OF ENGINEERING POTTALKULAM AZHAGAPPAPURAM P.O. KANYAKUMARI DISTRICT 629 401

ANNAI VAILANKANNI COLLEGE OF ENGINEERING
AVK Nagar, Pottalkulam, Azhagappapuram P.O, Kanyakumari District -629 401
ACADEMIC YEAR 2022-2023(EVEN)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INTERNAL ASSESSMENT TEST - 1
TIME TABLE

DATE	TIME	ECE		
		II YEAR	III YEAR	IV YEAR
15/03/2023	2.00 TO 3.30PM	EC3452 - Electromagnetic Fields	EC8691 – Microprocessors and Microcontrollers	GE8076 – Professional Ethics in Engineering
16/03/2023	2.00 TO 3.30PM	EC3401 - Networks and Security	EC8652 – Wireless Communication	EC8094 – Satellite Communication
18/03/2023	11.00 TO 12.30PM	EC3451 - Linear Integrated Circuits	MG8591 – Principles of management	-
	2.00 TO 3.30PM	EC3492 - Digital Signal Processing	EC8651 – Transmission Lines and RF Systems	-
20/03/2023	11.00 TO 12.30PM	EC3491 - Communication Systems	EC8095 – VLSI Design	-
	2.00 TO 3.30PM	GE3451 - Environamental Sciences and Sustainability	EC8002 – Multimedia Compression and Communication	-

TT Coordinator

HOD

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KANYAKUMARI DIST.

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ANNAI VAILANKANNI COLLEGE OF ENGINEERING
AVK Nagar, Pottalkulam, Azhagappapuram P.O, Kanyakumari District -629 401

ACADEMIC YEAR 2022-2023(EVEN)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INTERNAL ASSESSMENT TEST - 2
TIME TABLE

DATE	TIME	ECE		
		II YEAR	III YEAR	IV YEAR
17/04/2023	11.00 TO 12.30PM	EC3452 - Electromagnetic Fields	MG8591 – Principles of Management	-
	2.00 TO 3.30PM	EC3401 - Networks and Security	EC8095 – VLSI Design	EC8094 – Satellite Communication
18/04/2023	11.00 TO 12.30PM	EC3451 - Linear Integrated Circuits	EC8691 – Microprocessors and Microcontrollers	-
	2.00 TO 3.30PM	EC3492 - Digital Signal Processing	EC8651 – Transmission Lines and RF Systems	GE8076 – Professional Ethics in Engineering
19/04/2023	11.00 TO 12.30PM	EC3491 - Communication Systems	EC8002 – Multimedia Compression and Communication	-
	2.00 TO 3.30PM	GE3451 - Environmental Sciences and Sustainability	EC8652 – Wireless Communication	-

TT Coordinator

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ACADEMIC YEAR 2022-2023(EVEN)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
MODEL EXAMINATION
TIME TABLE

DATE	TIME	ECE		
		II YEAR	III YEAR	IV YEAR
15/05/2023	12.30 TO 03.30PM	EC3452 - Electromagnetic Fields	MG8591 – Principles of Management	-
16/05/2023	12.30 TO 03.30PM	EC3401 - Networks and Security	EC8095 – VLSI Design	EC8094 – Satellite Communication
17/05/2023	12.30 TO 03.30PM	EC3451 - Linear Integrated Circuits	EC8691 – Microprocessors and Microcontrollers	-
18/05/2023	12.30 TO 03.30PM	EC3492 - Digital Signal Processing	EC8651 – Transmission Lines and RF Systems	GE8076 – Professional Ethics in Engineering
19/05/2023	12.30 TO 03.30PM	EC3491 - Communication Systems	EC8002 – Multimedia Compression and Communication	-
22/05/2023	12.30 TO 03.30PM	GE3451 - Environmental Sciences and Sustainability	EC8652 – Wireless Communication	-

TT Coordinator

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AZHAGAPPAPURAM 629 401
KANYAKUMARI DIST.

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ANNAI VAILANKANNI COLLEGE OF ENGINEERING

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AVK Nagar, Pottalkulam, AzhagappapuramP.O.kanyakumari District–629 401

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

INTERNAL TEST-I

Subject Code/ Subject Name: EC8691 Microprocessors and Microcontrollers

Year/Branch : III ECE

Time: 2.00-3.30 PM
Date: 15/3/2023

Part: A(5*2=10)

Q.No	COs	Cognitive Level	Questions
1	CO1	K1	Draw the format of 8086 flag register
2	CO1	K1	What is linker?
3	CO1	K1	Calculate the physical address, when segment address is 10851H and effective address is 45371H.
4	CO2	K2	What is the operation of S0, S1 and S2 pins in maximum mode?
5	CO2	K4	In an 8086 microprocessor, the contents of the accumulator and the carry flag are A7 (in hex) and 0, respectively. If the instruction RLC is executed, then the contents of the accumulator (in hex) and the carry flag, respectively, will be------- (GATE-2016)

Part: B(2*16=32)

Q.No	COs	Cognitive Level	Questions
6(a)	CO1	K3	Explain the data transfer group and logical group of 8086 instructions
			OR
6(b)	CO1	K2	Explain the internal hardware architecture of 8086 microprocessor with neat diagram
7(a)	CO2	K3	Draw and explain the minimum mode of 8086
			OR
7(b)	CO2	K3	Explain closely coupled and loosely coupled configuration

Part: C(1*8=8)

Q.No	COs	Cognitive Level	Questions
8 (a)	CO1	K3	Explain different types of interrupts in 8086
			OR
8 (b)	CO2	K3	Write about coprocessor configuration

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ANNAI VAILANKANNI COLLEGE OF ENGINEERING

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AVK Nagar,, Pottalkualm, AzhagappapuramP.O.kanyakumari District–629 401

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

INTERNAL TEST-II

Subject Code/ Subject Name: EC8691 Microprocessors and Microcontrollers

Year/Branch : III ECE

Time: 11.00-12.30 PM

Date: 18/3/2023

Part: A(5*2=10)

Q.No	COs	Cognitive Level	Questions
1	CO3	K1	Mention the features of 8251 Serial Communication Interface
2	CO3	K1	Differentiate memory mapped I/O and I/O mapped I/O
3	CO4	K1	Write an ALP in 8051 to multiply the given number 55h and 87h. [Gate 2016]
4	CO4	K2	Write about BIT manipulation instructions of 8051.
5	CO4	K4	Write a program to add two 16 bit nos in 8051. The numbers are 4590 and 1234 . Store the sum in R7 and R6.

Part: B(2*16=32)

Q.No	COs	Cognitive Level	Questions
6(a)	CO3	K3	Explain in detail about serial communication interface-8251 with neat block diagram
			OR
6(b)	CO3	K3	Draw the functional block diagram of 8254 programmable interval timer and explain the different modes of operation.
7(a)	CO4	K3	With neat diagram explain the architecture of 8051 microcontroller
			OR
7(b)	CO4	K3	(i) Memory organization of 8051 (ii) Port P0 and P1 circuits

Part: C(1*8=8)

Q.No	COs	Cognitive Level	Questions
8 (a)	CO3	K3	Describe Traffic light controller interfacing .also write the program code.
			OR
8 (b)	CO4	K3	Illustrate the different addressing modes of 8051

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MODEL EXAMINATION

Subject Code: EC8551

Subject Name: COMMUNICATION NETWORKS

Time

Year/Branch :III/6

Part: A(5*2=10)

Q.No	COs	Cognitive Level	Questions
1	CO1	K1	Draw the flag register format of 8086 ?
2	CO1	K2	Calculate the physical address, when segment address is 1085 H and effective address is 4537 H.
3	CO2	K1	List the advanced microprocessors.
4	CO2	K1	What is main programming ? ?
5	CO3	K3	In an 8686 microprocessor, the contents of the accumulator and the carry flag are A7 (in hex) and 0,respectively . If the instruction RLC is executed ,then the contents of the accumulator (in hex) and the carry flag, respectively will be------(GATE-2016)
6	CO3	K1	List the four display modes of 8279 keyboard/ display controller
7	CO4	K1	Give the alternate function for the port pins of port 3?
8	CO4	K1	Name the special functions registers available in 8051?
9	CO5	K1	Which register is used for serial programming in 8051? Illustrate it.
10	CO5	K2	Which register is used for serial programming in 8056? Illustrate it

Part: B(5X13=65)

Q.No	COs	Cognitive Level	Questions
11(a)	CO1	K2	Explain the internal hardware architecture of 8086 microprocessor with neat diagram
			OR
11(b)	CO1	K2	Discuss the interrupts types of 8086 microprocessor?
12(a)	CO2	K3	Explain closely coupled and loosely coupled configuration?
			(or)
12(b)	CO3	K2	Draw and explain the minimum mode of 8086?

13(a)	CO3	K2	Explain D/A and A/D interfacing done with 8086 with an application.
			OR
13(b)	CO3	K2	Draw the functional mock diagram of 8254 timer and explain the different modes of operation
14(a)	CO4	K2	Explain the memory organization of 8051 microcontroller.
			OR
14(b)	CO4	K2	Draw the pin diagram of 8051 microcontroller and explain the function of pin.
15(a)	CO5	K2	Describe the difference modes of operation of timers/counters in 8051 with its associated register.
			OR
15(b)	CO5	K3	Draw the diagram to interface a stepper motor with 8051 microcontroller and explain. Write a 8051 assembly language program to run and the stepper motor in both forward and reverse direction with delay

Part: C(15X1=15)

Q.No	COs	Cognitive Level	Questions
16(a)	CO3	K3	Explain with neat block diagram the working of parallel communication interfacing chip.
			OR
16(b)	CO1	K4	(i) Write the assembly language program to transfer a block of data between memory locations. (ii) Write the assembly language program for counting the number of 1's in a register

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IAT I

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

AVK Nagar, Pottalkulam, Kanyakumari-629 401

Department of Electronics and Communication Engineering

IAT I

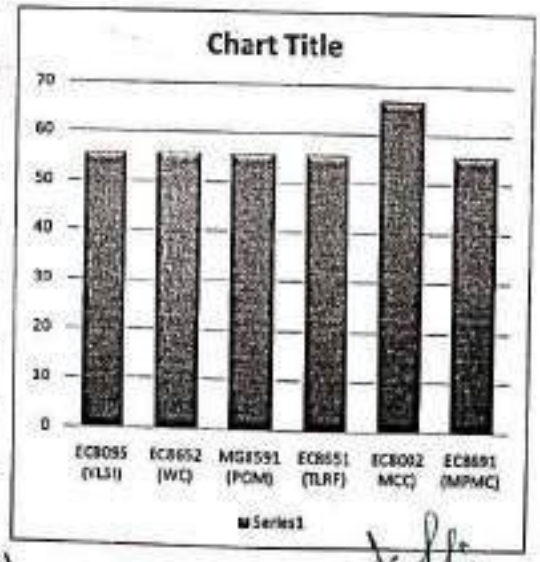
BATCH: 2020-2024 **YEAR: III** **STRENGTH: 9**

Sl.No.	Reg. Number	Name of the Student	Subject Code						Number of subjects Failed	Number of Subjects AB	% of Mark
			11-Sep	14-Sep	20-Sep	25-Sep	21-Sep	12-Sep			
			EC8095 (VLSI)	EC8652 (WC)	MG8591 (POM)	EC8651 (TLRF)	EC8002 MCC)	EC8691 (MPMC)			
1	960120106001	AHSAN AKTHAR A	24	6	32	40	61	40	5	-	Fail
2	960120106002	GANGA V	60	84	88	86	73	85	-	-	80
3	960120106003	GANGA DEVI M	56	82	90	72	64	66	-	-	72
4	960120106004	MAKENTH	AB	22	AB	50	24	25	3	2	AB
5	960120106005	SANTHIYA R	50	90	74	84	77	85	-	-	77
6	960120106006	SIVARAJ S	16	2	12	AB	AB	11	4	2	AB
7	960120106007	SREE VINISHA SHALINI P S	60	78	84	82	68	76	-	-	75
8	960120106008	THANUSHA T S	50	88	64	76	61	79	-	-	70
9	960120106306	SATHEESH KUMAR C	AB	20	AB	38	24	31	4	2	AB

Subject Code	EC8095 (VLSI)	EC8652 (WC)	MG8591 (POM)	EC8651 (TLRF)	EC8002 MCC)	EC8691 (MPMC)
No of Students Appeared	7	9	7	8	8	9
No of Students Failed	2	4	2	3	2	4
No of Students Absent	2	0	2	1	1	3
Total No. Of students	9	9	9	9	9	9
No of Students Passed	5	5	5	5	6	5
Pass Percentage	56	56	56	56	67	56

Total no.of Students	9
No of Students Passed in All Subjects	5
Overall Pass Percentage	55.6

Sl.No	SUBJECT CODE	NAME OF THE SUBJECT	FACULTY ALLOTED	% of Mark
1	EC8095 (VLSI)	VLSI Design	Mrs.E.Rajeswari	56
2	EC8652 (WC)	Wireless communication	Dr. Supriya	56
3	MG8591 (POM)	Principle of Management	Dr. Vinoth	56
4	EC8651 (TLRF)	Transmission Lines and RF Systems	Dr. Leonard Gibson	56
5	EC8002 MCC)	Multimedia Compression and Communication	Mr. R.Robert	67
6	EC8691 (MPMC)	Microprocessors and Microcontroller	Mrs.P.Renuka	56



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AVK Nagar, Pottalkulam, Kanyakumari-629 401

Department of Electronics and Communication Engineering

IAT II

BATCH: 2020-2024 **YEAR: III** **STRENGTH: 9**

Sl.No.	Reg. Number	Name of the Student	Subject Code						Number of subjects Failed	Number of Subjects AB	% of Mark
			12-Oct	10-Oct	11-Oct	11-Oct	12-Oct	10-Oct			
			EC8095 (VLSI)	EC8652 (WC)	MG8591 (POM)	EC8651 (TLRF)	EC8002 MCC)	EC8691 (MPMC)			
1	960120106001	ARSAN AKTHAR A	26	50	39	50	31	41	3	-	Fail
2	960120106002	GANGA V	76	84	82	78	88	66	-	-	95
3	960120106003	GANGA DEVI M	62	90	76	68	90	55	-	-	87
4	960120106004	HAKENTH	6	0	AB	0	AB	AB	3	2	AB
5	960120106005	SANTHIYA R	74	86	82	80	74	76	-	-	94
6	960120106006	SIVARAJ S	2	4	4	2	12	3	5	-	Fail
7	960120106007	SREE VINDHRA SHALINI P S	72	80	66	64	84	50	-	-	83
8	960120106008	THANUSHA T S	62	82	80	76	64	66	-	-	86
9	960120106106	SATHEESH KUMAR C	2	20	6	4	AB	9	5	-	Fail

Subject Code	EC8095 (VLSI)	EC8652 (WC)	MG8591 (POM)	EC8651 (TLRF)	EC8002 MCC)	EC8691 (MPMC)
No of Students Appeared	9	9	8	9	8	9
No of Students Failed	4	3	3	3	3	4
No of Students Absent	0	0	1	0	1	1
Total No. Of students	9	9	9	9	9	9
No of Students Passed	5	6	5	6	5	5
Pass Percentage	56	67	56	67	56	56

Total no of Students	9
No of Students Passed in All Subjects	5
Overall Pass Percentage	55.556

SLNo	SUBJECT CODE	NAME OF THE SUBJECT	FACULTY ALLOTED	% of Mark
1	EC8095 (VLSI)	VLSI Design	Mrs.E.Rajeswari	56
2	EC8652 (WC)	Wireless communication	Dr. Supriya	67
3	MG8591 (POM)	Principle of Management	Dr. Vinoth	56
4	EC8651 (TLRF)	Transmission Lines and RF Systems	Dr. Leonard Gibson	56
5	EC8002 MCC)	Multimedia Compression and Communication	Mr. K.Robert	67
6	EC8691 (MPMC)	Microprocessors and Microcontroller	Mrs.P.Renuka	56

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IAT 3

ANNAI VAILANKANNI COLLEGE OF ENGINEERING

AVK Nagar, Pottalkulam, Kanyakumari-629 401

Department of Electronics and Communication Engineering

IAT III

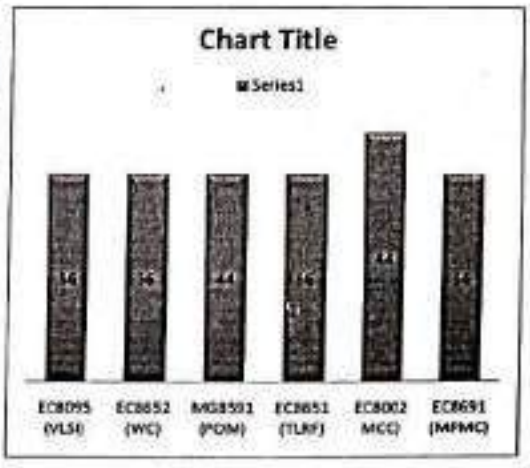
BATCH: 2020-2024 **YEAR: III** **STRENGTH: 9**

Sl.No.	Reg. Number	Name of the Student	Subject Code						Number of subjects Failed	Number of Subjects AB	% of Mark
			12-Oct	10-Oct	11-Oct	11-Oct	10-Oct	10-Oct			
			EC8095 (VLSI)	EC8652 (WC)	MG8591 (POM)	EC8651 (TLRF)	EC8002 MCC)	EC8691 (MPMC)			
1	960120106001	AHSAN AKTHAR A	50	38	68	52	50	51	1	-	Fail
2	960120106002	GANGA V	78	96	72	58	84	75	-	-	93
3	960120106003	GANGA DEVI M	AB	54	AB	AB	90	AB	-	4	AB
4	960120106004	MAKENTH	AB	AB	29	AB	0	AB	1	4	AB
5	960120106005	SANTHIYA R	74	84	62	72	86	80	-	-	92
6	960120106006	SIVAPAJ S	16	4	16	0	4	10	5	-	Fail
7	960120106007	SREE VINISHA SHALINI P S	66	80	56	62	80	72	-	-	83
8	960120106008	THANUSHA T S	58	58	AB	AB	82	AB	-	3	AB
9	960120106304	SATHEESH KUMAR C	AB	10	28	4	20	50	3	1	AB

Subject Code	EC8702 (AWSN)	EC8751 (OC)	EC8701 (AME)	EC8791 (ERTS)	OIE751 (Robotics)	EC8691 (MPMC)
No of Students Appeared	9	9	8	9	8	9
No of Students Failed	1	3	3	2	1	4
No of Students Absent	3	1	2	3	3	3
Total No. Of students	9	9	9	9	9	9
No of Students Passed	5	5	4	4	5	5
Pass Percentage	56	56	44	44	56	56

Total no.of Students	9
No of Students Passed in All Subjects	3
Overall Pass Percentage	33.33

Sl.No.	SUBJECT CODE	NAME OF THE SUBJECT	FACULTY ALLOTED	% of Mark
1	EC8095 (VLSI)	VLSI Design	Mrs.E.Rajeswari	56
2	EC8652 (WC)	Wireless communication	Dr. Supriya	56
3	MG8591 (POM)	Principle of Management	Dr. Vinoth	44
4	EC8651 (TLRF)	Transmission Lines and RF Systems	Dr. Leonard Gibson	56
5	EC8002 MCC)	Multimedia Compression and Communication	Mr. R.Robert	44
6	EC8691 (MPMC)	Microprocessors and Microcontroller	Mrs.P.Renuka	56



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Department of Electronics and Communication Engineering

6th Sem University Exam Result Analysis

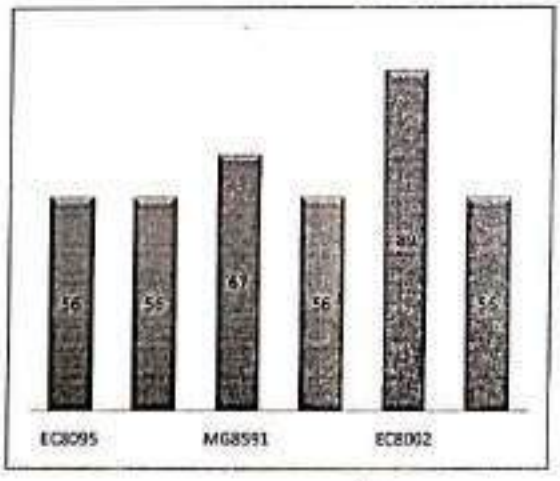
BATCH: 2020-2024 **YEAR: III / 6** **STRENGTH: 09**

Sl.No.	Reg. Number	Name of the Student	Subject Code						Number of subjects Failed	Number of Subjects AB	Number of Sub.Pass
			EC8095 (VLSI)	EC8652 (WC)	MG8591(POM)	EC8651 (TRF)	EC8002 (MCC)	EC8691 (MPMC)			
1	960120106001	AHSAN AKTHAR A	U	B	B+	U	A	U	3		3
2	960120106002	GANGA V	B	A	B+	B	A+	B+	-	-	6
3	960120106003	GANGA DEVI M	B	A	B+	B	A	B+			6
4	960120106004	MAKENTH	U	UA	U	U	UA	UA	3	3	0
5	960120106005	SANTHIYA R	B	A	B+	B	A+	B+	-	-	6
6	960120106006	SIVARAJ S	U	UA	U	U	B	UA	3	2	1
7	960120106007	SREE VINISHA SHALINI P S	B+	B	B+	B	B+	B+	-	-	6
8	960120106008	THANUSHA T S	B	U	B	B	A	B	1		5
9	960120106306	SATHEESH KUMAR C	U	U	U	U	B	U	5	-	1

Subject Code	EC8095	EC8652	MG8591	EC8651	EC8002	EC8691
No of Students Appeared	9	7	9	9	8	7
No of Students Failed	4	2	3	4	0	2
No of Students Absent	0	2	0	0	1	2
Total No. Of students	9	9	9	9	9	9
No of Students Passed	5	5	6	5	8	5
Pass Percentage	56	56	67	56	89	56

Total no.of Students	9
No of Students Passed in All Subjects	4
Overall Pass Percentage	44.4

Sl.No	SUBJECT CODE	NAME OF THE SUBJECT	FACULTY ALLOTED	% of Mark
1	EC8095 (VLSI)	VLSI Design	Mrs.E.Rajeswari	56
2	EC8652 (WC)	Wireless Communication	Dr. Supriya	56
3	MG8591 (POM)	Principles of Management	Dr.Vinoth	67
4	EC8651 (TRF)	Transmission Lines and RF Systems	Dr.Leonard Gibson	56
5	EC8002 (MCC)	Multimedia Compression and Communication	Mr.R.Robert	89
6	EC8691 (MPMC)	Microprocessors and Microcontrollers	Mrs.P.Renuka	56



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Department of Electronics & Communication Engineering

COURSE OUTCOME ATTAINMENT

Subject Code/ Name:	EC8691 / Microprocessors and Microcontr	Staff Name	Mrs.P.Renuka	Batch :	2020-2024
Year/Sem :	II/6	Benchmark (%)		Number of Students in Class:	12

Sl.No	Register Number	Name of the Student	Qn. No.	Part A					Part B						* CO Attainment (100%)		Number of Students Attained	Number of Students Attained
				1	2	3	4	5	6		7		8					
			Sub Div.						a	b	a	b	a	b				
			Courses	CO1	CO1	CO1	CO2	CO2	CO1	CO1	CO1	CO1	CO2	CO1				
			Ind Mark	2	2	2	2	2	16	16	16	16	10	10	CO AD8501.1	CO AD8501.2	CO AD8501.1	CO AD8501.2
1	960120106001	AHSAN AKTHAR A	26	1		2		1		10		12			66	8	N	N
2	960120106002	GANGA V	24	1	1		1		8		8		5		47	50	N	N
3	960120106003	GANGA DEVI M	24	2		1	1			10		5	5		47	50	N	N
4	960120106004	MAKENTH R	4	2	2										11	0	N	N
5	960120106005	SANTHIYA R	31		2		2		12		10		5		63	58	N	N
6	960120106006	SIVARAJ S	5	2	2								5		11	42	N	N
7	960120106007	SREE VINESHA SHALINI P.S	31		2	2			12		10		5		68	42	N	N
8	960120106009	THANUSHA T.S	28	1		1		2		10				5	32	58	N	N
9	960120106303	BELWIN JOSHUA J	14				2	2	10						26	33	N	N
10	960120106305	KARTHICK	11	1			1				10				29	8	N	N
11	960120106306	SATHESSKUMAR C	17		1		1				10		5		29	50	N	N
12	960120106308	SUNDAR RAJA P	11		2		2			5			2		18	33	N	N
															Number of Students attained More than 60% of Marks		0	0
															% of CO Attainment		0.00	0.00
															attainment Level		0	0

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Department of Electronics & Communication Engineering

COURSE OUTCOME ATTAINMENT

INTERNAL ASSESSMENT II

Subject Code/ Name:	EC3601 / Microprocessors and Micr	Staff Name	Mrs.P.Renuka	Batch :	2020-2024
Year/Sem:	III/6	Benchmark %	[redacted]	Number of Students in Class:	12

Sl.No	Register Number	Name of the Student	Q.No	Part A					Part B						CO Attainment (100%)		Number of Students Attained	Number of Students Attained
				1	2	3	4	5	6		7		8					
			Sub Div						a	b	a	b	a	b				
			Outcome	CO2	CO2	CO3	CO3	CO3	CO2	CO2	CO3	CO3	CO3	CO3				
			Ltd Mark	2	2	2	2	2	10	10	10	10	10	10	CO AD8501.2	CO AD8501.3	CO AD8501.2	CO AD8501.3
1	960120106001	AHSAN AKTHAR A	29	2		1	1		10		10		5		60	57	N	N
2	960120106002	GANGA V	25		2	1		1		5		10		6	35	60	N	N
3	960120106003	GANGA DEVI M	31	2		2	2	2		8		12	3		50	70	N	N
4	960120106004	MAKENTH R	7				1	1					5		0	23	N	N
5	960120106005	SANTHIYA R	30	2		2	2	1	10		5		8		60	60	N	N
6	960120106006	SIVARAJ S	8	1	1	1				5					35	3	N	N
7	960120106007	SREE VINISHA SHALINI R.C	33		2		2	2		10		12		5	60	70	N	N
8	960120106009	THANUSHA T.S	23		1	2	2		10					8	55	40	N	N
9	960120106301	BELWIN JOSHUA J	31	2		2			12		10		5		70	57	N	N
10	960120106305	KARTHICK	14		2		2		10						60	7	N	N
11	960120106306	SATHESSKUMAR C	33	1		1	1			10					55	7	N	N
12	960120106308	SUNDAR RAJA P	18	1		1		1			10		5		5	57	N	N
															Number of Students attained More than 80% of Marks		0	0
															% of CO Attainment		0.00	0.00
															attainment Level		0	0

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COURSE OUTCOME ATTAINMENT

INTERNAL ASSESSMENT III

Subject Code/ Name:	EC8691 / Microprocessors and Microcontrollers	Staff Name:	Mrs.P.Renuka	Batch :	2020-2024
Year/Sem :	III/6	Benchmark %	[redacted]	Number of Students in Class:	12

Sl.No	Register Number	Name of the Student	50	Part A					Part B						Attainment(100%)		Number of Students Attained	Number of Students Attained
			Q.No.	1	2	3	4	5	6		7		8					
			Sub Div						a	b	a	b	a	b				
			Outcome	CO4	CO4	CO4	CO5	CO5	CO4	CO4	CO5	CO6	CO6	CO5				
			IA3 Mark	2	2	2	2	2	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	CO AD8501.4	CO AD8501.5	CO AD8501.4	CO AD8501.5
1	960120106001	AHSAN AKTHAR A	31	2		2		2	10		10		5		64	61	N	N
2	960120106002	GANGA V	35	2	2		1			12		10		8	73	68	N	N
3	960120106003	GANGA DEVI M	29	1		2	2	1		10		8	5		59	57	N	N
4	960120106004	MAKENTH R	6	1		1								4	9	14	N	N
5	960120106005	SANTHIYA R	34	2	2	2	1	1	10		8			8	73	64	N	N
6	960120106006	SIVARAJ S	11		1	1	1							8	9	32	N	N
7	960120106007	SREE VINISHA SHALINI P.S	36		2	2	2	1		12		12	5		73	71	N	N
8	960120106009	JHANUSHA T.S	19	1	1	1	1				10		5		14	37	N	N
9	960120106303	BELWIN JOSHUA J	26	2	2			2	10		10				64	43	N	N
10	960120106305	KARTHICK	12					2			5		5		0	43	N	N
11	960120106306	SATHESSKUMAR C	18		1			2	5		10				27	43	N	N
12	960120106308	SUNDAR RAJA P	12			1	1				10				5	39	N	N

Number of Students attained More than 80% of Marks	0	0
% of CO Attainment	0.00	0.00
Attainment Level	0	0

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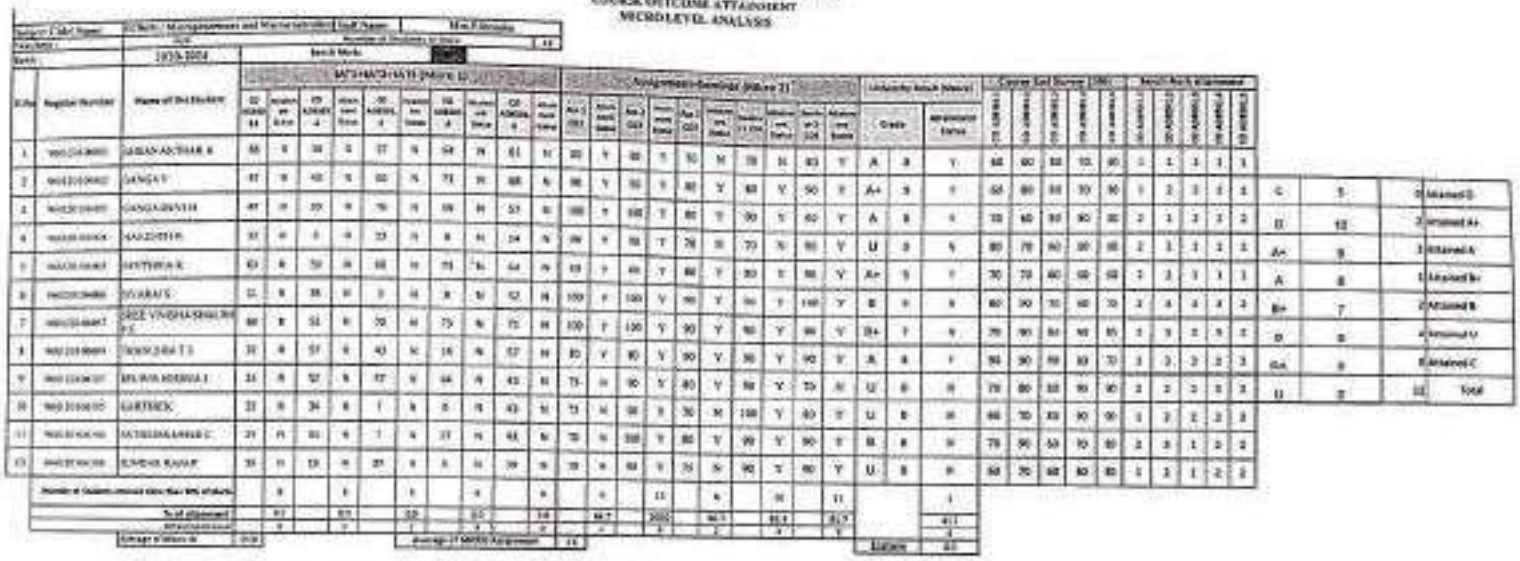
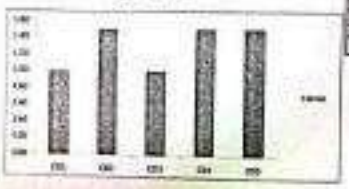
COURSE OUTCOME ATTAINMENT

MICRO LEVEL ANALYSIS





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PO-CO MAPPING

	SUBJECT CODE &	/ Microprocessors and Microcon			
BATCH	YEAR		BRANCH	ECE	
ACADEMIC YEAR	2022-2023				

OVERALL CO ATTAINMENT	0.62

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
1	2	2	2	1	0	0	0	0	0	0	0	0	1	2
2	3	2	2	1	0	0	0	0	0	0	0	0	1	2
3	3	2	2	1	0	0	0	0	0	0	0	0	1	2
4	3	2	2	1	0	0	0	0	0	0	0	0	1	2
5	3	2	2	1	0	0	0	0	0	0	0	0	1	2
CO	2.80	2.00	2.00	1.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	1.00	2.00

PO-CO ATTAINMENT

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
1	0.41	0.41	0.41	0.21	0	0	0	0	0	0	0	0	0.21	0.41
2	0.62	0.41	0.41	0.21	0	0	0	0	0	0	0	0	0.21	0.41
3	0.62	0.41	0.41	0.21	0	0	0	0	0	0	0	0	0.21	0.41
4	0.62	0.41	0.41	0.21	0	0	0	0	0	0	0	0	0.21	0.41
5	0.62	0.41	0.41	0.21	0	0	0	0	0	0	0	0	0.21	0.41
CO	0.58	0.61	0.41	0.21	0	0	0	0	0	0	0	0	0.21	0.41

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Date: 16 /03/2023

CIRCULAR FOR FIRST CLASS COMMITTEE MEETING

The First class committee meeting for the III-year ECE (6TH SEM) is scheduled on 17.03.2023 at 10.40 A.M in Simulation Lab. The following staff and students have to attend the meeting without fail.

CHAIR PERSON	Dr.Abilash
CONVENER	Mrs.P.Renuka
CLASS COORDINATOR	Mrs.E.Rajeswari
STAFF MEMBERS	Dr.Leonard Gibson
	Dr.A.Narendra Kumar
	Dr.Saheer Abubacker
	Dr.Supriya
	Dr.Vinoth
	Mr.R.Robert
STUDENT MEMBERS	A.Ahsan Akthar
	R.Santhiya

CHAIR PERSON

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Minutes of III Year Class Committee Meeting-I

Department of Electronics and Communication Engineering

Date of Meeting: 17-03-2023 **Time: 10.40 A.M-11.00A.M**

Members Present

1.Dr.Abilash , Professor/ECE	:	Chair Person
2.Mrs.P.Renuka , HoD, ECE	:	Convener
3.Mrs.E.Rajeswari AP/ECE	:	Class coordinator
4.Dr.Leonard Gibson Professor /ECE	:	Member
5.Dr.A.Narendra Kumar ,ASP/ECE	:	Member
6.Dr.Saheer Abubacker.ASP/ECE	:	Member
7. Dr.Supriya ASP/ECE	:	Member
8. Dr.Vinoth	:	Member
9.Mr.R.Robert	:	Member
10. A.Ahsan Akthar	:	Student Representative
11 R.Santhiya	:	Student Representative

The following matters were discussed in the meeting

1. The Students were instructed to be punctual for the class and maintain proper dress code.
2. The Student's feedback was received regarding the subjects.
3. The Students were asked to intimate their inconvenience to their concerned class coordinator.
4. The Students were advised to make use of seminar classes and placement hours effectively for improving their skills.
5. The Students were advised to be attentive in classes as well as laboratory classes.

HOD

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(Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai)

AVK Nagar,, Pottalkualm, AzhagappapuramP.O.kanyakumari District–629 401

Date: 17/03 /2023

ATTENDANCE OF CLASS COMMITTEE MEETING-I

The following staff and students have attended the meeting on 17/03/2023.

S.NO.	NAME OF MEMBERS	SIGNATURE
1	Dr.Abilash	
2	Mrs.P.Renuka	
3	Mrs.E.Rajeswari	
4	Dr.Leonard Gibson	
5	Dr.A.Narendra Kumar	
6	Dr.Saheer Abubacker	
7	Dr.Supriya	
8	Dr.Vinoth	
9	Mr.R.Robert	

HOD/ECE

17/3/23.

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Date: 19 /04 /2023

CIRCULAR FOR CLASS COMMITTEE MEETING-II

The second class committee meeting for the III-year ECE (6TH SEM) is scheduled on 21.4.2023 at 10.40 A.M in Simulation Lab. The following staff and students have to attend the meeting without fail.

CHAIR PERSON	Dr.Abilash
CONVENER	Mrs.P.Renuka
CLASS COORDINATOR	Mrs.E.Rajeswari
STAFF MEMBERS	Dr.Leonard Gibson
	Dr.A.Narendra Kumar
	Dr.Saheer Abubacker
	Dr.Supriya
	Dr.Vinoth
	Mr.R.Robert
STUDENT MEMBERS	A.Ahsan Akthar
	R.Santhiya

CHAIR PERSON

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MEMBERS

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Minutes of III Year Class Committee Meeting-II

Department of Electronics and Communication Engineering

Date of Meeting: 21-04-2023 **Time: 10.40 A.M-11.00A.M**

Members Present

1.Dr.Abilash , Professor/ECE	:	Chair Person
2.Mrs.P.Renuka , HoD, ECE	:	Convener
3.Mrs.E.Rajeswari AP/ECE	:	Class coordinator
4.Dr.Leonard Gibson Professor /ECE	:	Member
5.Dr.A.Narendra Kumar ,ASP/ECE	:	Member
6.Dr.Saheer Abubacker.ASP/ECE	:	Member
7. Dr.Supriya ASP/ECE	:	Member
8. Dr.Vinoth	:	Member
9.Mr.R.Robert	:	Member
10. A.Ahsan Akthar	:	Student Representative
11 R.Santhiya	:	Student Representative

The following matters were discussed in the meeting

1.Internal Assessment _I result analysis was discussed in the meeting.
2.The Student's feedback was received regarding the subjects and Lab.
3.Retest is decided for the absentees of IAT-I .
4.The Students were advised to make use of seminar classes and placement hours effectively for improving their skills.
5.The students are advised to keep their classrooms and surrounding clean.
6. Students are encouraged to participate in conferences and workshops.

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Date: 21/04 /2023

ATTENDANCE OF CLASS COMMITTEE MEETING-II

The following staff and students have attended the meeting on 21/04/2023.

S.NO.	NAME OF MEMBERS	SIGNATURE
1	Dr.Abilash	
2	Mrs.P.Renuka	
3	Mrs.E.Rajeswari	
4	Dr.Leonard Gibson	
5	Dr.A.Narendra Kumar	
6	Dr.Saheer Abubacker	
7	Dr.Supriya	
8	Dr.Vinoth	
9	Mr.R.Robert	

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21/4/23

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Date: 16 /05 /2023

CIRCULAR FOR CLASS COMMITTEE MEETING-III

The third class committee meeting for the III-year ECE (6TH SEM) is scheduled on 19.5.2023 at 10.40 A.M in Simulation Lab. The following staff and students have to attend the meeting without fail.

CHAIR PERSON	Dr.Abilash
CONVENER	Mrs.P.Renuka
CLASS COORDINATOR	Mrs.E.Rajeswari
STAFF MEMBERS	Dr.Leonard Gibson
	Dr.A.Narendra Kumar
	Dr.Saheer Abubacker
	Dr.Supriya
STUDENT MEMBERS	Dr.Vinoth
	Mr.R.Robert
	A.Ahsan Akthar
	R.Santhiya

CHAIR PERSON

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MEMBERS

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Minutes of II Year Class Committee Meeting-III

Department of Electronics and Communication Engineering

Date of Meeting: 19-05-2023 **Time: 10.40 A.M-11.00A.M**

Members Present

1.Dr.Abilash , Professor/ECE	:	Chair Person
2.Mrs.P.Renuka , HoD, ECE	:	Convener
3.Mrs.E.Rajeswari AP/ECE	:	Class coordinator
4.Dr.Leonard Gibson Professor /ECE	:	Member
5.Dr.A.Narendra Kumar ,ASP/ECE	:	Member
6.Dr.Saheer Abubacker.ASP/ECE	:	Member
7. Dr.Supriya ASP/ECE	:	Member
8. Dr.Vinoth	:	Member
9.Mr.R.Robert	:	Member
10. A.Ahsan Akthar	:	Student Representative
11 R.Santhiya	:	Student Representative

The following matters were discussed in the meeting

1. Internal Assessment _2 result analysis was discussed in the meeting.
2. The Student's feedback was received regarding the subjects and Lab.
3. HoD enquired about the completion of lab experiments and records.
4. It was decided in the meeting to provide question bank with answers for all subjects.

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Date: 19/05 /2023

ATTENDANCE OF CLASS COMMITTEE MEETING-III

The following staff and students have attended the meeting on 19/05/2023.

S.NO.	NAME OF MEMBERS	SIGNATURE
1	Dr.Abilash	
2	Mrs.P.Renuka	
3	Mrs.E.Rajeswari	
4	Dr.Leonard Gibson	
5	Dr.A.Narendra Kumar	
6	Dr.Saheer Abubacker	
7	Dr.Supriya	
8	Dr.Vinoth	
9	Mr.R.Robert	

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19/5/23

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